TX8X

Computer On Module

- Processor — ARM® Cortex®-A35 based NXP i.MX 8X Series
- RAM — 1GB DDR3L SDRAM
- ROM — 4GB eMMC
- Power supply — 3.3V to 5V
- Size — 31mm SO-DIMM
- Grade — Industrial
- Temperature — -25°C to 85°C

Quad Cortex®-A35

Key Features

- Cortex-A35
  - Lowest power ARMv8-A CPU
- ECC Capabilities
  - L1 cache parity
  - L2 cache ECC
- Display support:
  - Combo MIPI DSI / LVDS interfaces
  - Vivante GC7000 Series GPU
- Camera Interfaces:
  - 4-lane MIPI CSI2
  - 1x parallel 8-bit CSI (BT.656)
- Cortex-M4 core for real-time processing

Connectivity

- 10/100Mbps Ethernet
- 2x USB, 2x CAN
- 4x UART, 8x I²C, 4x SPI
- PCIe 3.0 (1-lane)
- 3.3V I/O

OS Support

- Linux

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)
www.karo-electronics.de

Computer on module

Extending the scalable range of the i.MX 8 series, the i.MX 8X family is comprised of common subsystems and architecture from the higher-end i.MX 8 family, establishing an unmatched range of cost-performance scaling with pin-compatible options and the highest level of software reuse. Built with a high-level integration to support graphics, video, image processing, audio, and voice functions, the i.MX 8X processor family is ideal for safety-certifiable and efficient performance requirements. Example applications include industrial automation & control, HMI, robotics, building control, automotive cluster, display audio, infotainment, and telematics applications.

The TX8X is a member of the TXCOM module series, specially designed for i.MX multimedia processors. TXCOM modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. With a focus on longevity TXCOM modules includes an i.MX processor, power supply and memory.

- NXP i.MX 8QuadXPlus, 1GB DDR3L SDRAM
- 4GB eMMC
- DIMM200-module (67,6mm x 31 mm x 4mm)
- Operation temperature up to 105°C (processor junction temp.)

Standard TXCOM pinout:

Highly scalable design options allow a single platform to cover multiple products. Pin-compatible TX modules allow a single PCB as a platform for different features as product needs dictate.

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces (x2)
- 4-wire SD-Card/SDIO

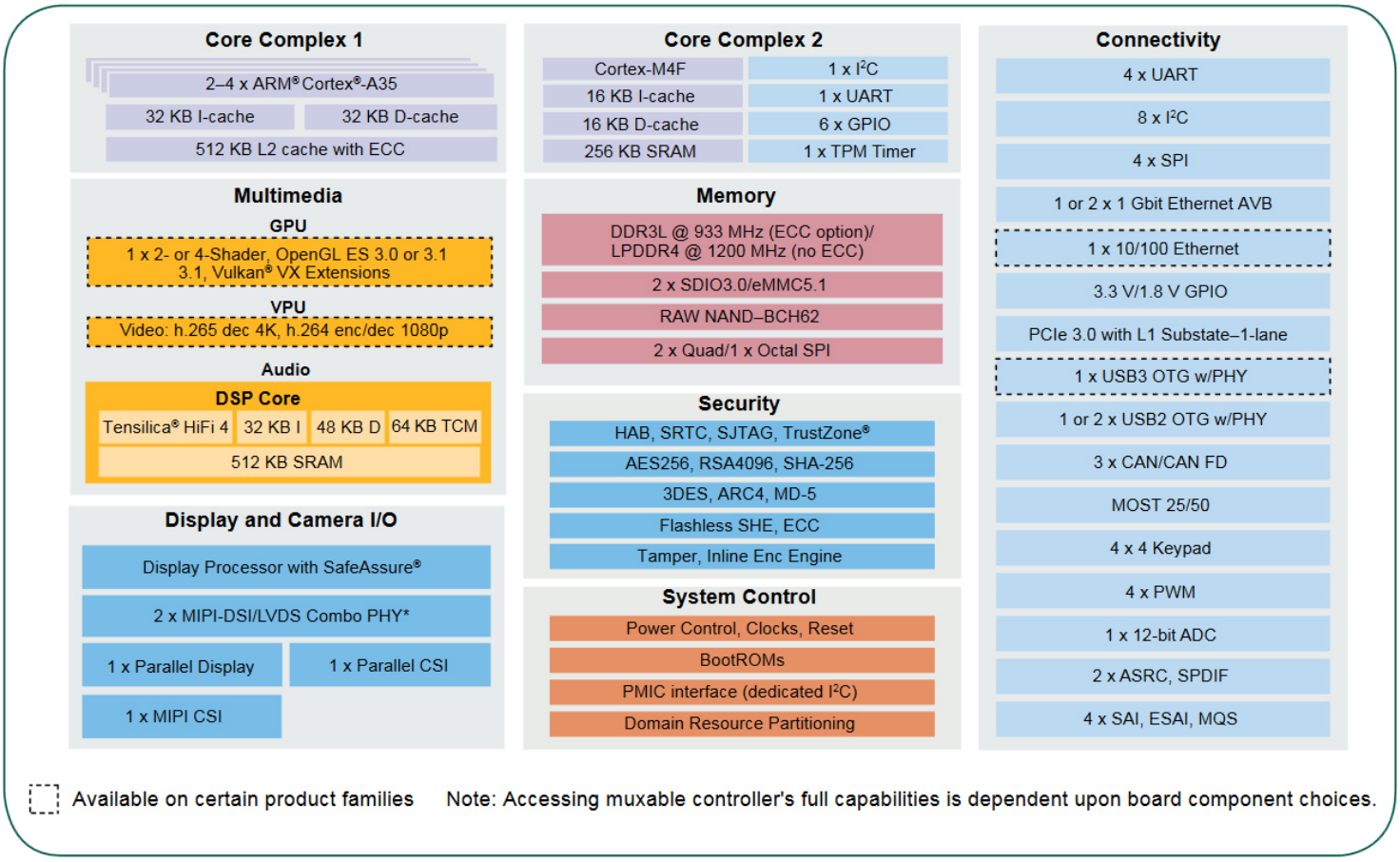
High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide

i.MX 8X FAMILY BLOCK DIAGRAM



* Each single PHY can either be a 1× 4 lane MIPI-DSI or a 1×1 channel LVDS interface for a total of 2 display interfaces. In combination, the two PHYs can be configured to be a single 2-channel LVDS interface.

Ordering Information

Order Number	CPU	SDRAM	Flash	GPU	VPU	USB 3.0
TX8XQP/1024S/4GF/E85	i.MX 8QuadXPlus Quad Core Industrial	1GB 32-bit DDR3L	4GB	GC7000 Lite	4K h.265 dec 1080p h.264	yes

2018-09-27

PINOUT

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input.
5-7, 9-12	power	VOUT				3.3V power supply output. Supplied by SW7
8	3V3	BOOTMODE				Boot mode select H: Boot from eMMC / L: Boot from UART/USB
13	power	VBACKUP				
14						
15	3V3	#RESET_OUT	USDHC1_RESET_B	NAND.RE_N SPI2.SCK	GPIO4[19]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime.
16		#POR				Power On Reset — Active low input signal Leave unconnected, if not used.
17		#RESET_IN				
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	USB_SS3_TC1	I2C1.SCL **USB_OTG2.PWR**	GPIO4[04]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	USB_SS3_TC3	I2C1.SDA **USB_OTG2.OC**	GPIO4[06]	Active low over-current indicator input connected to a GPIO.
29	analog	USBH_DM	**USB_OTG2_DN**			D- pin of the USB cable
30	analog	USBH_VBUS	**USB_OTG2_VBUS**			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
31	analog	USBH_DP	**USB_OTG2_DP**			D+ pin of the USB cable
32	GND	GND				
USB-OTG						
33	3V3	USBOTG_ID	**USB_OTG1_ID**			
34	3V3	USBOTG_VBUSEN	USB_SS3_TC0	I2C1.SCL **USB_OTG1.PWR** USB_OTG2.PWR	GPIO4[03]	Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	**USB_OTG1_DN**			D- pin of the USB cable
36	3V3	#USBOTG_OC	USB_SS3_TC2	I2C1.SDA **USB_OTG1.OC** USB_OTG2.OC	GPIO4[05]	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	**USB_OTG1_DP**			D+ pin of the USB cable
38	analog	USBOTG_VBUS	**USB_OTG1_VBUS**			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND				

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
I2C						
40	3V3	I2C_DATA	**MIPI_DSI0_I2C0_SDA**	MIPI_DSI1.GPIO0.IO03	GPIO1[26]	I2C Data
41	3V3	I2C_CLK	**MIPI_DSI0_I2C0_SCL**	MIPI_DSI1.GPIO0.IO02	GPIO1[25]	I2C Clock
PWM						
42	3V3	PWM	MIPI_DSI0_GPIO0_00	I2C1.SCL MIPI_DSI0.PWM0.OUT	GPIO1[27]	PWM Output
1-WIRE						
43	3V3	OWDAT	MIPI_DSI0_GPIO0_01	I2C1.SDA	GPIO1[28]	
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	**SPI0_CS0**	SAI0.RXD M40.TPM0.CH1 M40.GPIO0.IO03	GPIO1[08]	Slave Select (Selectable polarity) signal
45	3V3	CSPI_SS	QSPI0A_SS1_B		GPIO3[15]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	**SPI0_SDO**	SAI0.TXFS M40.I2C0.SDA M40.GPIO0.IO01	GPIO1[06]	Master Out/Slave In signal
47	3V3	CSPI_MISO	**SPI0_SDI**	SAI0.TXD M40.TPM0.CH0 M40.GPIO0.IO02	GPIO1[05]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	**SPI0_SCK**	SAI0.TXC M40.I2C0.SCL M40.GPIO0.IO00	GPIO1[04]	Serial Clock signal
49	3V3	CSPI_RDY	CSI_EN	CSI_I2C.SCL I2C3.SCL SPI1.SDI	GPIO3[02]	Serial Data Ready signal
50	GND	GND				
SD – Secure Digital Interface 1						
51	3V3	SD1_CD	**USDHC1_CD_B**	NAND.DQS_P SPI2.CS0 NAND.DQS	GPIO4[22]	SD Card Detect
52	3V3	SD1_D[0]	**USDHC1_DATA0**	NAND.CE1_B MQS.L	GPIO4[25]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	3V3	SD1_D[1]	**USDHC1_DATA1**	NAND.RE_B UART3.TX	GPIO4[26]	
54	3V3	SD1_D[2]	**USDHC1_DATA2**	NAND.WE_B UART3.CTS_B	GPIO4[27]	
55	3V3	SD1_D[3]	**USDHC1_DATA3**	NAND.ALE UART3.RTS_B	GPIO4[28]	
56	3V3	SD1_CMD	**USDHC1_CMD**	NAND.CE0_B MQS.R	GPIO4[24]	SD Command bidirectional signal
57	3V3	SD1_CLK	**USDHC1_CLK**	UART3.RX	GPIO4[23]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	TXD	**UART0_TX**	MQS.L FLEXCAN0.TX	GPIO1[22]	Application UART 1 Transmit Data output signal
60	3V3	RXD	**UART0_RX**	MQS.R FLEXCAN0.RX	GPIO1[21]	Application UART 1 Receive Data input signal
61	3V3	RTS	FLEXCAN0_RX	SAI2.RXC UART0.RTS_B SAI1.TXC	GPIO1[15]	Application UART 1 Request to Send **input** signal
62	3V3	CTS	FLEXCAN0_TX	SAI2.RXD UART0.CTS_B SAI1.TXFS	GPIO1[16]	Application UART 1 Clear to Send **output** signal
2nd UART						
63	3V3	TXD	**UART1_TX**	PWM0.OUT GPT0.CAPTURE	GPIO0[21]	Application UART 2 Transmit Data output signal
64	3V3	RXD	**UART1_RX**	PWM1.OUT GPT0.COMPARE GPT1.CLK	GPIO0[22]	Application UART 2 Receive Data input signal
65	3V3	RTS	**UART1_RTS_B**	PWM2.OUT LCD_D16 GPT1.CAPTURE GPT0.CLK		Application UART 2 Request to Send **input** signal
66	3V3	CTS	**UART1_CTS_B**	PWM3.OUT LCD_D17	GPIO0[24]	Application UART 2 Clear to Send **output** signal

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
				GPT1.COMPARE		
3rd UART						
67	3V3	TXD	**UART2_TX**	FTM.CH1 FLEXCAN1.TX	GPIO1[23]	Application UART 3 Transmit Data output signal
68	3V3	RXD	**UART2_RX**	FTM.CH0 FLEXCAN1.RX	GPIO1[24]	Application UART 3 Receive Data input signal
69	3V3	RTS	FLEXCAN2_TX	SAI3.RXFS UART3.TX SAI1.RXC	GPIO1[20]	
70	3V3	CTS	FLEXCAN2_RX	SAI3.RXD UART3.RX SAI1.RXFS	GPIO1[19]	
71	GND	GND				
KEYPAD / 1st CAN						
72	3V3	KP_COL[0]	QSPI0B_SCLK	QSPI1A.SCLK **KPP0.COL0**	GPIO3[17]	
73	3V3	KP_COL[1]	QSPI0B_DATA0	QSPI1A.DATA0 **KPP0.COL1**	GPIO3[18]	
74	3V3	KP_COL[2]	QSPI0B_DATA1	QSPI1A.DATA1 **KPP0.COL2**	GPIO3[19]	
75	3V3	KP_COL[3]	QSPI0B_DATA2	QSPI1A.DATA2 **KPP0.COL3**	GPIO3[20]	
76	3V3	TXCAN	**FLEXCAN1_TX**	SAI3.RXC DMA0.REQ_IN0 SAI1.RXD	GPIO1[18]	
77	3V3	KP_ROW[0]	QSPI0B_DATA3	QSPI1A.DATA3 **KPP0.ROW0**	GPIO3[21]	
78	3V3	KP_ROW[1]	QSPI0B_DQS	QSPI1A.DQS **KPP0.ROW1**	GPIO3[22]	
79	3V3	KP_ROW[2]	QSPI0B_SS0_B	QSPI1A.SS0_B **KPP0.ROW2**	GPIO3[23]	
80	3V3	KP_ROW[3]	QSPI0B_SS1_B	QSPI1A.SS1_B **KPP0.ROW3**	GPIO3[24]	
81	3V3	RXCAN	**FLEXCAN1_RX**	SAI2.RXFS FTM.CH2 SAI1.TXD	GPIO1[17]	
82	GND	GND				
SSI 1 - Serial Audio Port 1						
83	3V3	SSI1_INT	PCIE_CTRL0_PERST_B		**GPIO4[00]**	
84	3V3	SSI1_RXD	**SAI0_RXD**	SAI1.RXFS SPI1.CS0 LCD_D20	GPIO0[27]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	**SAI0_TXD**	SAI1.RXC SPI1.SDO LCD_D18	GPIO0[25]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	**SAI0_TXC**	SAI1.TXD SPI1.SDI LCD_D19	GPIO0[26]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	**SAI0_TXFS**	SPI2.CS1 SPI1.SCK	GPIO0[28]	Serial Audio Interface left/right clock
88	GND	GND				
SSI 2 - Serial Audio Port 2						
89	3V3	SSI2_INT	PCIE_CTRL0_WAKE_B		**GPIO4[02]**	
90	3V3	SSI2_RXD	**SAI1_RXD**	SAI0.RXFS SPI1.CS1 LCD_D21	GPIO0[29]	Serial Audio Interface serial data line 1
91	3V3	SSI2_TXD	SPI0_CS1	SAI0.RXC **SAI1.TXD** LCD_PWM0	GPIO1[07]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	**SAI1_RXC**	SAI1.TXC LCD_D22	GPIO0[30]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	**SAI1_RXFS**	SAI1.TXFS LCD_D23	GPIO0[31]	Serial Audio Interface left/right clock
94	GND	GND				

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
Quad SPI						
95	3V3		QSPI0A_SS0_B		GPIO3[14]	
96	3V3		QSPI0A_DATA0		GPIO3[09]	
97	3V3		QSPI0A_DATA1		GPIO3[10]	
98	3V3		QSPI0A_DATA2		GPIO3[11]	
99	3V3		QSPI0A_DATA3		GPIO3[12]	
100	3V3		QSPI0A_DQS		GPIO3[13]	
101	3V3		QSPI0A_SCLK		GPIO3[16]	
102	GND	GND				
CMOS Sensor Interface						
103	3V3	CSI0_DAT12	**CSI_D00**	CI_PI.CSI_D02 ADMA.SAI0.RXC SNVS.TAMPER_OUT0		
104	3V3	CSI0_DAT13	**CSI_D01**	CI_PI.CSI_D03 ADMA.SAI0.RXD SNVS.TAMPER_OUT1		
105	3V3	CSI0_DAT14	**CSI_D02**	CI_PI.CSI_D04 ADMA.SAI0.RXFS SNVS.TAMPER_OUT2		
106	3V3	CSI0_DAT15	**CSI_D03**	CI_PI.CSI_D05 ADMA.SAI2.RXC SNVS.TAMPER_OUT3		
107	3V3	CSI0_DAT16	**CSI_D04**	CI_PI.CSI_D06 ADMA.SAI2.RXD SNVS.TAMPER_OUT4		
108	3V3	CSI0_DAT17	**CSI_D05**	CI_PI.CSI_D07 ADMA.SAI2.RXFS SNVS.TAMPER_IN0		
109	3V3	CSI0_DAT18	**CSI_D06**	CI_PI.CSI_D08 ADMA.SAI3.RXC SNVS.TAMPER_IN1		
110	3V3	CSI0_DAT19	**CSI_D07**	CI_PI.CSI_D09 ADMA.SAI3.RXD SNVS.TAMPER_IN2		
111	GND	GND				
112	3V3	CSI0_HSYNC	**CSI_HSYNC**	CI_PI.CSI_D00 ADMA.SAI3.RXFS SNVS.TAMPER_IN3		
113	3V3	CSI0_VSYNC	**CSI_VSYNC**	CI_PI.CSI_D01 SNVS.TAMPER_IN4		
114	3V3	CSI0_PIXCLK	**CSI_MCLK**	MIPI_CSI0.I2C0.SDA ADMA.SPI1.SDO	GPIO3[01]	
115	3V3	CSI0_MCLK	**CSI_PCLK**	MIPI_CSI0.I2C0.SCL ADMA.SPI1.SCK	GPIO3[00]	

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
116	GND	GND				
LCD Controller						
117	LVDS		**MIPI_DSI0_DATA2_N**			
118	LVDS		**MIPI_DSI0_DATA1_N**			
119	LVDS		**MIPI_DSI0_DATA2_P**			
120	LVDS		**MIPI_DSI0_DATA1_P**			
121	LVDS		**MIPI_DSI0_DATA3_N**			
122	LVDS		**MIPI_DSI0_DATA0_N**			
123	LVDS		**MIPI_DSI0_DATA3_P**			
124	LVDS		**MIPI_DSI0_DATA0_P**			
125	LVDS		**MIPI_DSI0_CLK_N**			
126	LVDS		**MIPI_DSI1_DATA3_P**			
127	LVDS		**MIPI_DSI0_CLK_P**			
128	LVDS		**MIPI_DSI1_DATA3_N**			
129	GND	GND				
130	LVDS		**MIPI_DSI1_CLK_P**			
131	LVDS		**MIPI_DSI1_DATA2_P**			
132	LVDS		**MIPI_DSI1_CLK_N**			
133	LVDS		**MIPI_DSI1_DATA2_N**			
134	LVDS		**MIPI_DSI1_DATA1_P**			
135	LVDS		**MIPI_DSI1_DATA0_P**			
136	LVDS		**MIPI_DSI1_DATA1_N**			
137	LVDS		**MIPI_DSI1_DATA0_N**			
138	LVDS		USB_SS3_RX_N			
139	LVDS		USB_SS3_TX_N			
140	LVDS		USB_SS3_RX_P			
141	LVDS		USB_SS3_TX_P			
142	GND	GND				
143	3V3	HSYNC	SPI3_CS0	ACM.MCLK_OUT1 **LCD_HSYNC**	GPIO0[16]	
144	3V3	VSYNC	MCLK_IN0	ESAI0.RX_HF_CLK **LCD_VSYNC** SPI2.SDI	GPIO0[19]	
145	3V3	OE_ACD	MCLK_IN1	I2C3.SDA **LCD_EN** SPI2.SCK LCD_D17		
146	3V3	LSCLK	MCLK_OUT0	ESAI0.TX_HF_CLK **LCD_CLK** SPI2.SDO	GPIO0[20]	

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
147	GND	GND				
Module Specific Signals						
148	3V3		ESAI0_FSR	ENET1.RCLK50M_OUT LCD_D00 ENET1.RGMII_TXC ENET1.RCLK50M_IN		
149	3V3		ESAI0_FST	MLB.CLK LCD_D01 ENET1.RGMII_TXD2	GPIO0[01]	
150	3V3		ESAI0_SCKR	LCD_D02 ENET1.RGMII_TX_CTL	GPIO0[02]	
151	3V3		ESAI0_SCKT	MLB.SIG LCD_D03 ENET1.RGMII_TXD3	GPIO0[03]	
152	3V3		ESAI0_TX0	MLB.DATA LCD_D04 ENET1.RGMII_RXC	GPIO0[04]	
153	3V3		ESAI0_TX1	LCD_D05 ENET1.RGMII_RXD3	GPIO0[05]	
154	3V3		ESAI0_TX2_RX3	ENET1.RMII_RX_ER LCD_D06 ENET1.RGMII_RXD2	GPIO0[06]	
155	3V3		ESAI0_TX3_RX2	LCD_D07 ENET1.RGMII_RXD1	GPIO0[07]	
156	3V3		ESAI0_TX4_RX1	LCD_D08 ENET1.RGMII_TXD0	GPIO0[08]	
157	3V3		ESAI0_TX5_RX0	LCD_D09 ENET1.RGMII_TXD1	GPIO0[09]	
158	3V3		SPDIF0_RX	MQS.R LCD_D10 ENET1.RGMII_RXD0	GPIO0[10]	
159	3V3		SPDIF0_TX	MQS.L LCD_D11 ENET1.RGMII_RX_CTL	GPIO0[11]	
160	GND	GND				
161	3V3		SPDIF0_EXT_CLK	LCD_D12 ENET1.REFCLK_125M_25M	GPIO0[12]	
162	3V3		SPI3_CS1	I2C3.SCL LCD_RESET SPI2.CS0 LCD_D16		
163	3V3		SPI3_SCK	LCD_D13	GPIO0[13]	
164	3V3		SPI3_SDI	LCD_D15	GPIO0[15]	
165	3V3		SPI3_SDO	LCD_D14	GPIO0[14]	

PIN	Type	Function	i.MX8X Pad Name	Alternate functions	GPIO	Description (refer to i.MX8X Dual manuals for details)
166	LVDS		PCIE_REFCLK100M_N			
167	LVDS		PCIE0_RX0_N			
168	LVDS		PCIE_REFCLK100M_P			
169	LVDS		PCIE0_RX0_P			
170	LVDS		PCIE0_TX0_N			
171	GND	GND				
172	LVDS		PCIE0_TX0_P			
173	3V3		MIPI_DSI1_GPIO0_00	I2C2.SCL MIPI_DSI1.PWM0.OUT	GPIO1[31]	
174	3V3		MIPI_DSI1_GPIO0_01	I2C2.SDA	GPIO2[00]	
175	3V3		MIPI_DSI1_I2C0_SCL	MIPI_DSI0.GPIO0.IO02	GPIO1[29]	
176	3V3		MIPI_DSI1_I2C0_SDA	MIPI_DSI0.GPIO0.IO03	GPIO1[30]	
177	3V3		PCIE_CTRL0_CLKREQ_B		GPIO4[01]	
178	1V8		ADC_IN0	M40.I2C0.SCL M40.GPIO0.IO00	GPIO1[10]	
179	1V8		ADC_IN1	M40.I2C0.SDA M40.GPIO0.IO01	GPIO1[09]	
180	1V8		ADC_IN2	M40.UART0.RX M40.GPIO0.IO02 ACM.MCLK_IN0	GPIO1[12]	
181	1V8		ADC_IN3	M40.UART0.TX M40.GPIO0.IO03 ACM.MCLK_OUT0	GPIO1[11]	
182	1V8		ADC_IN4	M40.TPM0.CH0 M40.GPIO0.IO04	GPIO1[14]	
183	GND	GND				
184	1V8		ADC_IN5	M40.TPM0.CH1 M40.GPIO0.IO05	GPIO1[13]	
185	1V8		MIPI_CSI0_GPIO0_00	I2C0.SCL	GPIO3[08]	
186	1V8		MIPI_CSI0_GPIO0_01	I2C0.SDA	GPIO3[07]	
187	1V8		MIPI_CSI0_I2C0_SCL	MIPI_CSI0.GPIO0.IO02	GPIO3[05]	
188	1V8		MIPI_CSI0_I2C0_SDA	MIPI_CSI0.GPIO0.IO03	GPIO3[06]	
189	LVDS		MIPI_CSI0_DATA3_N			
190	1V8		MIPI_CSI0_MCLK_OUT		GPIO3[04]	
191	LVDS		MIPI_CSI0_DATA3_P			
192	LVDS		MIPI_CSI0_DATA1_N			
193	LVDS		MIPI_CSI0_CLK_N			
194	LVDS		MIPI_CSI0_DATA1_P			
195	LVDS		MIPI_CSI0_CLK_P			
196	LVDS		MIPI_CSI0_DATA0_N			
197	LVDS		MIPI_CSI0_DATA2_P			
198	LVDS		MIPI_CSI0_DATA0_P			
199	LVDS		MIPI_CSI0_DATA2_N			
200	GND	GND				