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FDS4141_F085

P-Channel PowerTrench® MOSFET

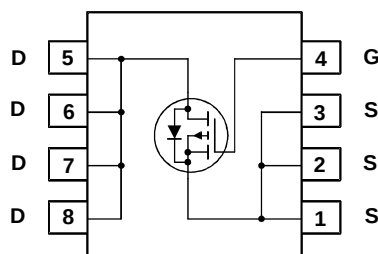
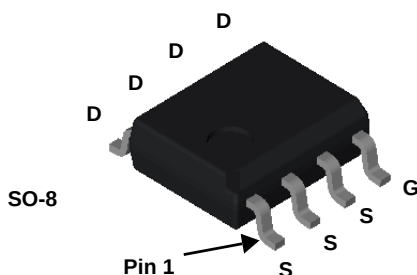
-40V, -10.8A, 19.0mΩ

Features

- Typ $r_{DS(on)}$ = 10.5mΩ at $V_{GS} = -10V$, $I_D = -10.5A$
- Typ $r_{DS(on)}$ = 14.8mΩ at $V_{GS} = -4.5V$, $I_D = -8.4A$
- Typ $Q_{g(TOT)}$ = 35nC at $V_{GS} = -10V$
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Control switch in synchronous & non-synchronous buck
- Load switch
- Inverter



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10\text{V}$)	-10.8	A
	Pulsed	-36	
E_{AS}	Single Pulse Avalanche Energy	229	mJ
P_D	Power Dissipation	1.6	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	30	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient SO-8, 1in^2 copper pad area	81	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS4141	FDS4141_F085	SO-8	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -32\text{V}$,	-	-	-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$,	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1.0	-1.7	-3.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = -10.5\text{A}, V_{GS} = -10\text{V}$	-	10.5	13.0	m Ω
		$I_D = -8.4\text{A}, V_{GS} = -4.5\text{V}$	-	14.8	19.0	
		$I_D = -10.5\text{A}, V_{GS} = -10\text{V}$, $T_J = 125^\circ\text{C}$	-	15.3	19.0	
g_{FS}	Forward Transconductance	$I_D = -10.5\text{A}, V_{DD} = -5\text{V}$		34		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} = 0V, f = 1MHz		-	2005	-	pF
C _{oss}	Output Capacitance			-	355	-	pF
C _{rss}	Reverse Transfer Capacitance			-	190	-	pF
R _g	Gate Resistance	f = 1MHz		-	5.0	-	Ω
Q _{g(TOT)}	Total Gate Charge at -10V	V _{GS} = 0 to -10V	V _{DD} = -20V I _D = -10.5A	-	35	45	nC
Q _{g(-5)}	Total Gate Charge at -5V	V _{GS} = 0 to -5V		-	18.6	24.2	nC
Q _{gs}	Gate to Source Gate Charge			-	5.2	-	nC
Q _{gd}	Gate to Drain “Miller” Charge			-	6.6	-	nC

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = -20\text{V}, I_D = -10.5\text{A}$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	-	-	25	ns
$t_{d(on)}$	Turn-On Delay Time		-	9.7	-	ns
t_r	Rise Time		-	4.4	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	41	-	ns
t_f	Fall Time		-	11.6	-	ns
t_{off}	Turn-Off Time		-	-	84	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = -10.5\text{A}$	-	-0.8	-1.3	V
		$I_{SD} = -2.1\text{A}$	-	-0.7	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -10.5\text{A}, d_{SD}/dt = 100\text{A}/\mu\text{s}$	-	26	34	ns
Q_{rr}	Reverse Recovery Charge		-	13.4	17.4	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 6.2\text{mH}$, $I_{AS} = -8.6\text{A}$

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Typical Characteristics

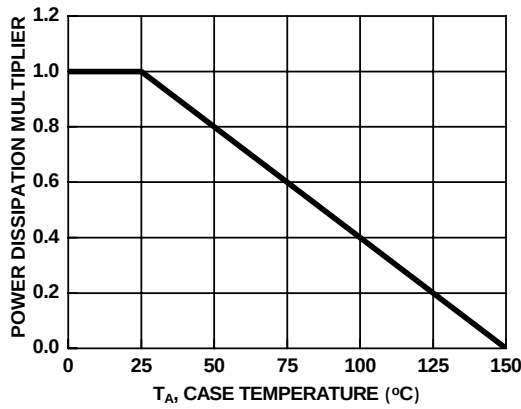


Figure 1. Normalized Power Dissipation vs Ambient Temperature

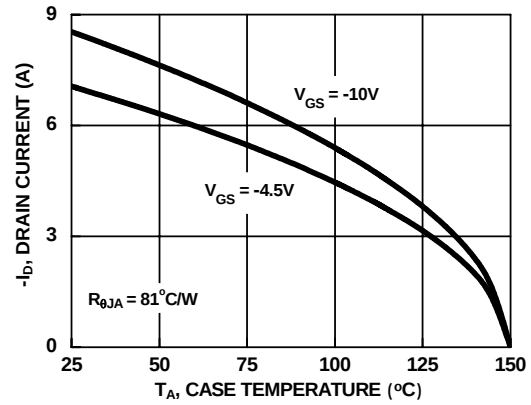


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

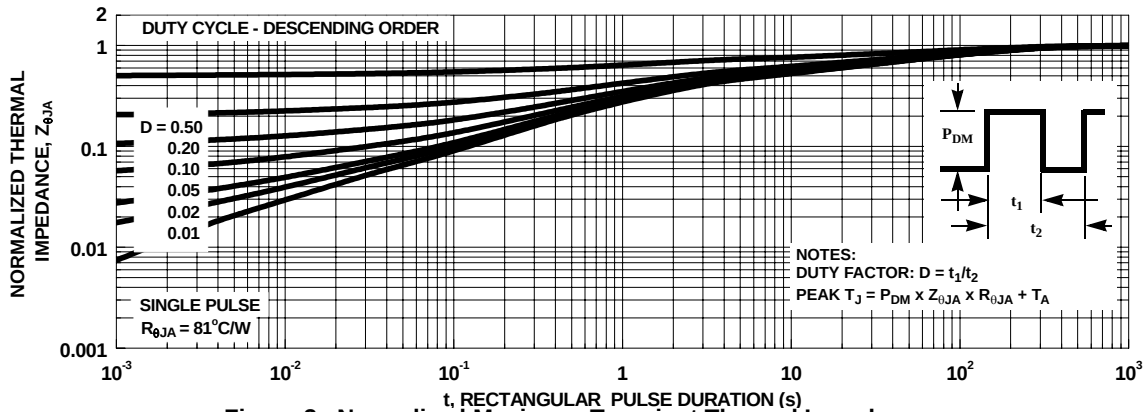


Figure 3. Normalized Maximum Transient Thermal Impedance

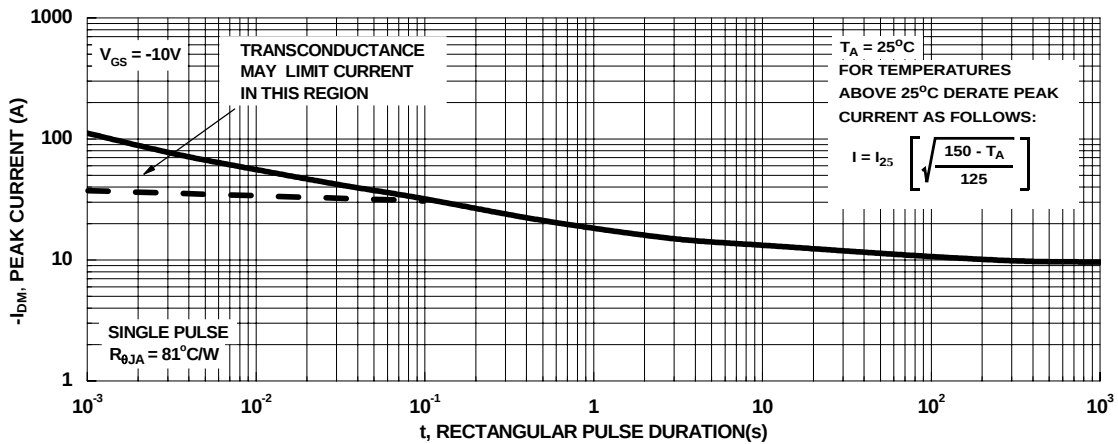


Figure 4. Peak Current Capability

Typical Characteristics

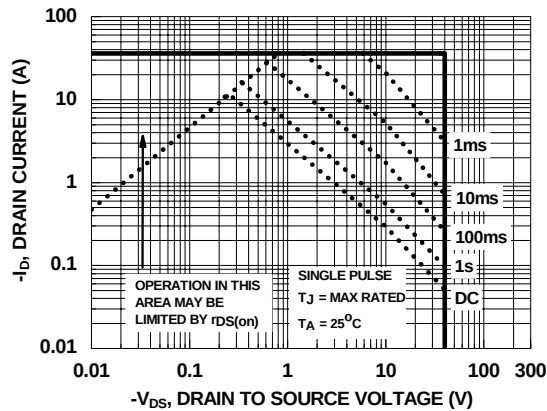
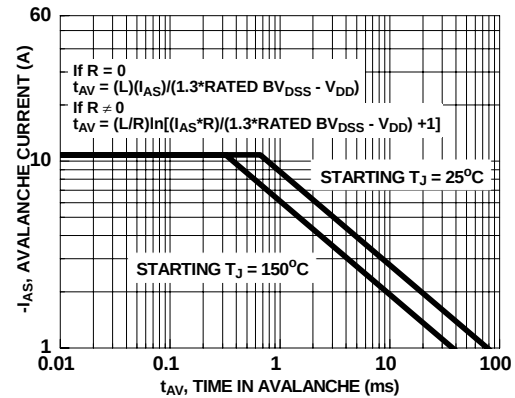


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

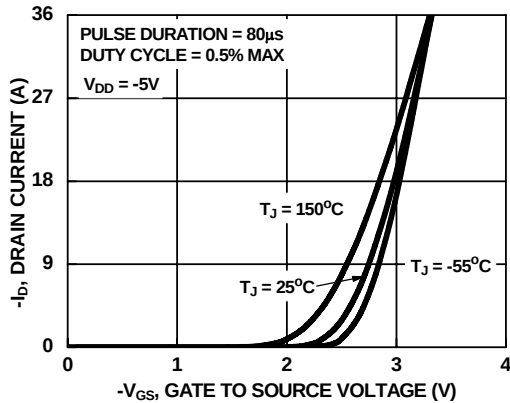


Figure 7. Transfer Characteristics

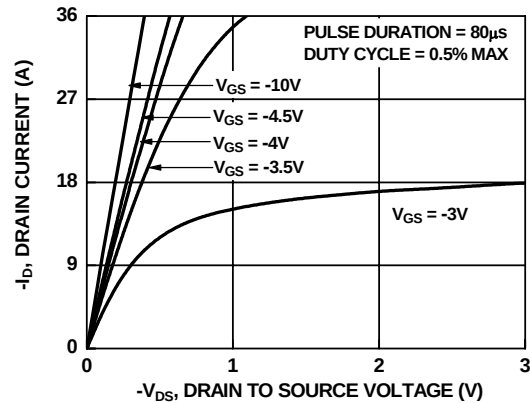


Figure 8. Saturation Characteristics

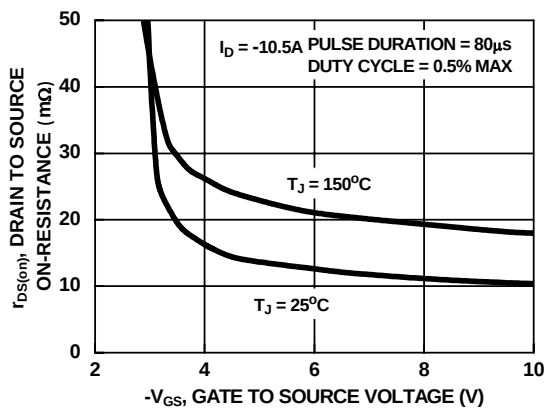


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

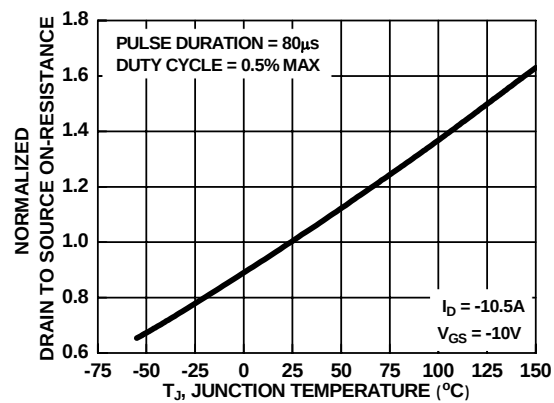


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

Typical Characteristics

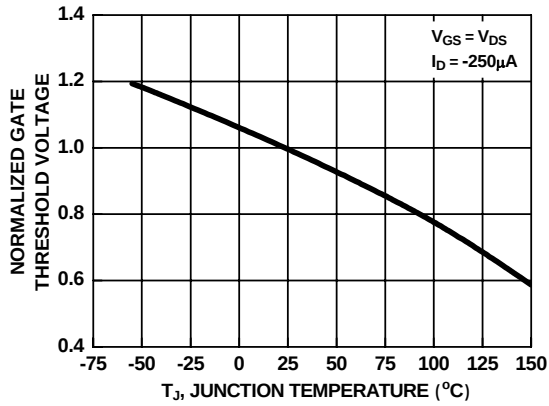


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

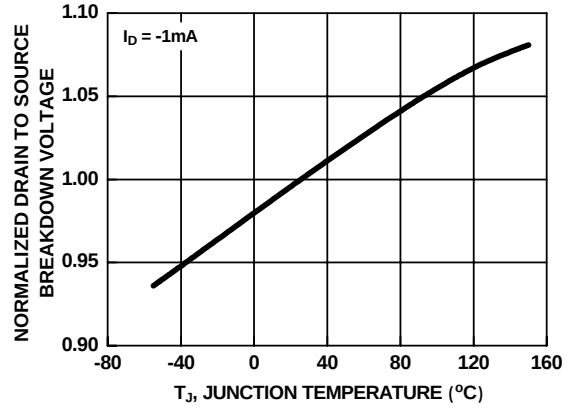


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

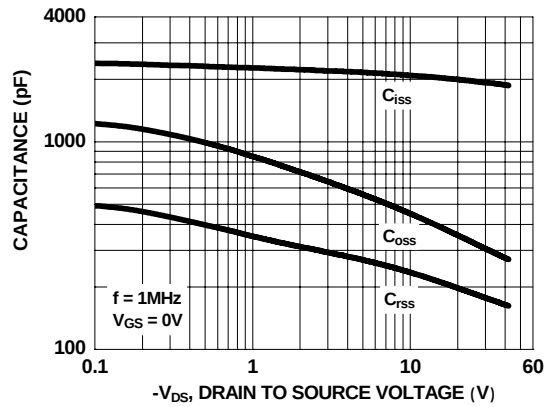


Figure 13. Capacitance vs Drain to Source Voltage

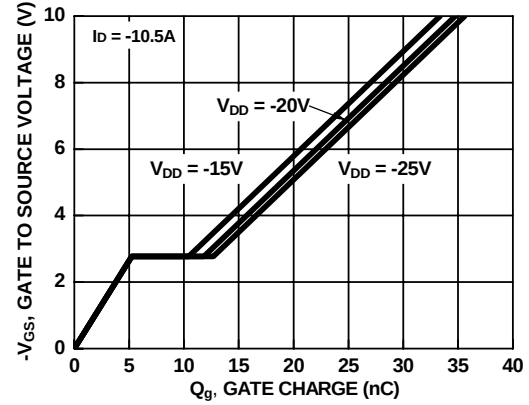
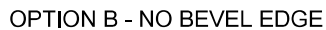
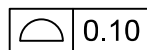
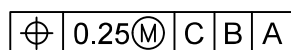


Figure 14. Gate Charge vs Gate to Source Voltage



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16

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