LNK40x2-40x4
LinkSwitch-4 Family

Energy-Efficient, Accurate Primary-Side Regulated
CV/CC Switcher for Adapters and Chargers

Product Highlights

Dramatically Simplifies CV/CC Converters
- Eliminates optocoupler and all secondary CV/CC control circuitry
- Eliminates all control loop compensation circuitry

Advanced Performance Features
- Dynamic base drive technology provides flexibility in choice of BJT transistor by dynamically optimizing BJT switching characteristics
  - Extends RBSOA of BJT
  - Dramatically reduces sensitivity to BJT gain
- Compensates for transformer inductance tolerances
- Compensates for input line voltage variations
- Compensates for cable voltage drop
- Compensates for external component temperature variations
- Very accurate IC parameter tolerances using proprietary trimming technology
- Frequency up to 65 kHz to reduce transformer size
- The minimum peak current is fixed to improve transient load response

Advanced Protection/Safety Features
- Single fault output overvoltage and short-circuit
- Over-temperature protection

EcoSmart™– Energy Efficient
- Meets DoE 6 and CoC V5 2016 via an optimized quasi-resonant switching PWM/PFM control
- No-load consumption of <30 mW at 230 VAC input

Green Package
- Halogen free and RoHS compliant package

Applications
- Chargers for cell/cordless phones, PDAs, MP3/portable audio devices, adapters, etc.

Description

The LinkSwitch™-4 family of ICs dramatically simplifies low power CV/CC charger design by eliminating an optocoupler and secondary control circuitry. The LinkSwitch-4 family adaptive BJT drive technology uses combined base and emitter switching to boost switching performance and deliver higher efficiency, wider Reverse Bias Safe Operating Area (RBSOA) margin and the flexibility to accommodate a wide range of low cost BJT. The device incorporates a multimode PWM/PFM controller with quasi resonant switch to maximize the efficiency, meet <30 mW no-load and at same time maintain fast transient response greater than 4.3 V with a load change from 0% to 100%.

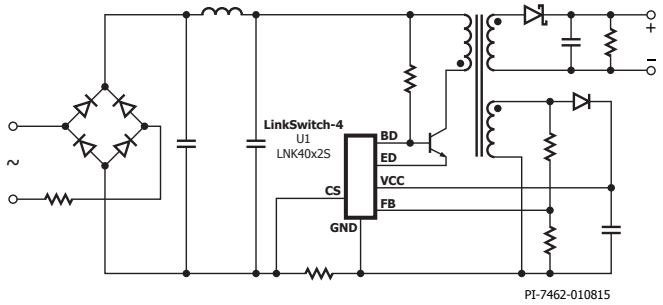


Figure 1. Typical Application (SOT-23-6) (S).

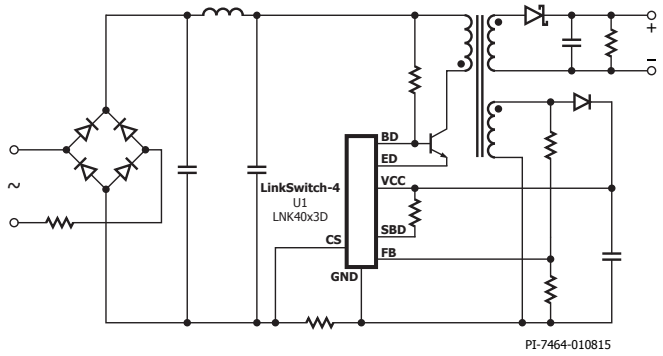


Figure 2. Typical Application (SO-8) (D).

Output Power Table

Product[3,4]	85 - 265 VAC	
	Adapter[1]	Open Frame[2]
LNK40x2S	6.5 W	6.5 W
LNK40x3S	8 W	8 W
LNK40x3D	10 W	10 W
LNK40x4D	15 W	15 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient, device T_J ≤ 100 °C.
2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at +50 °C.
3. Package: D: SO-8 , S: SOT-23-6.
4. Cable compensation factor. x = 0 (no cable compensation), x = 1 (3% cable compensation) x = 2 (6% cable compensation).

Figure 3. SOT-23-6 and SO-8 Packages.

This Product is Covered by Patents and/or Pending Patent Applications.

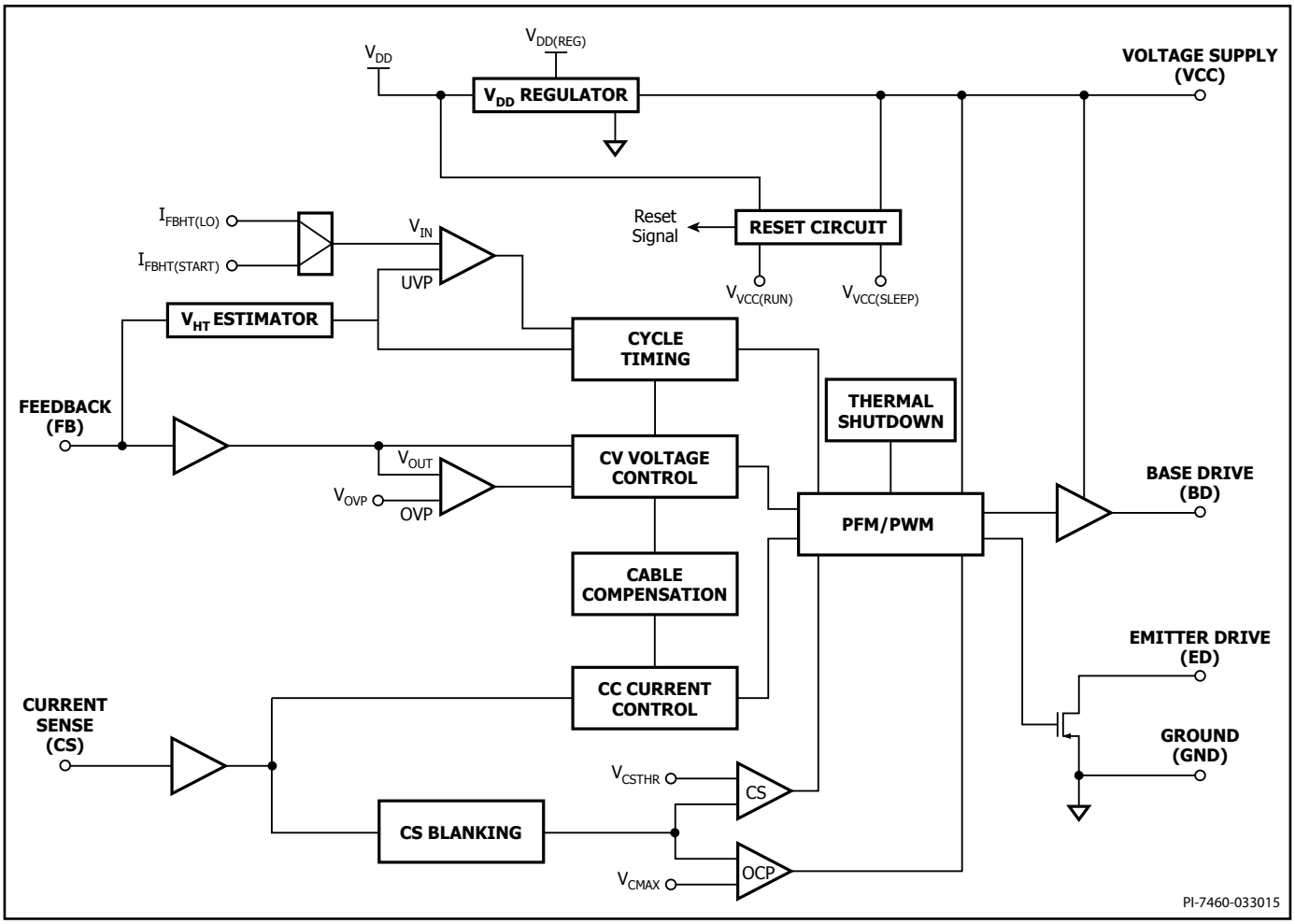


Figure 4. LNK40x2S Functional Block Diagram.

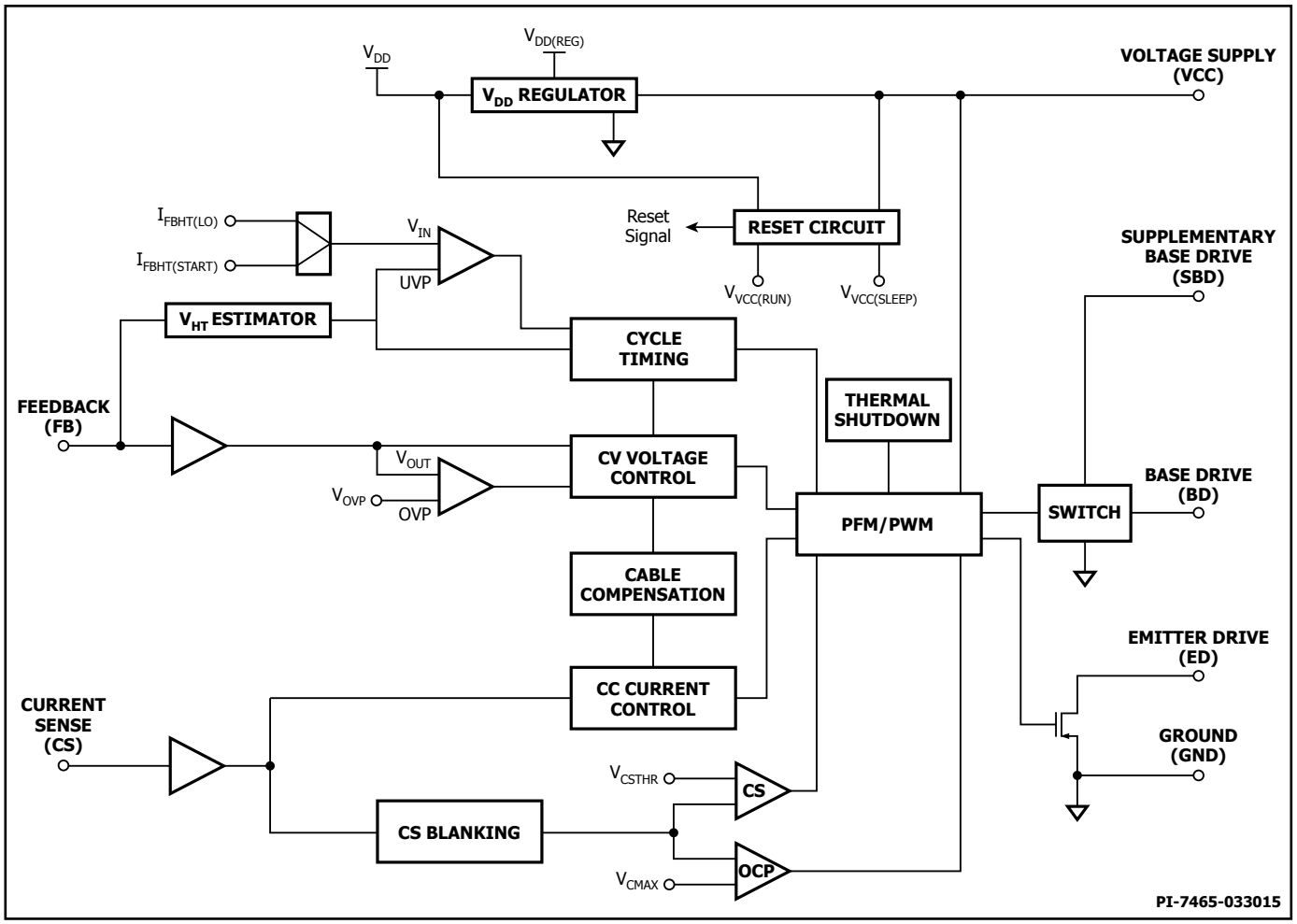


Figure 5. LNK40x3D Functional Block Diagram.

Pin Functional Description

VOLTAGE SUPPLY (VCC) Pin:
During Run mode, power derived from the transformer voltage supply winding is fed to the control circuitry via the VOLTAGE SUPPLY pin.

BASE DRIVE (BD) Pin:
BASE DRIVE pin for BJT.

EMITTER DRIVE (ED) Pin:
EMITTER DRIVE pin for BJT.

FEEDBACK (FB) Pin:
The FEEDBACK pin input provides feedback to the control circuitry by monitoring the transformer voltage waveform.

GROUND (GND) Pin:
Power and signal ground.

Primary CURRENT SENSE (CS) Pin:
Primary CURRENT SENSE pin via R_{CS}.

SUPPLEMENTARY BASE DRIVE (SBD) Pin:
Supplementary base drive.

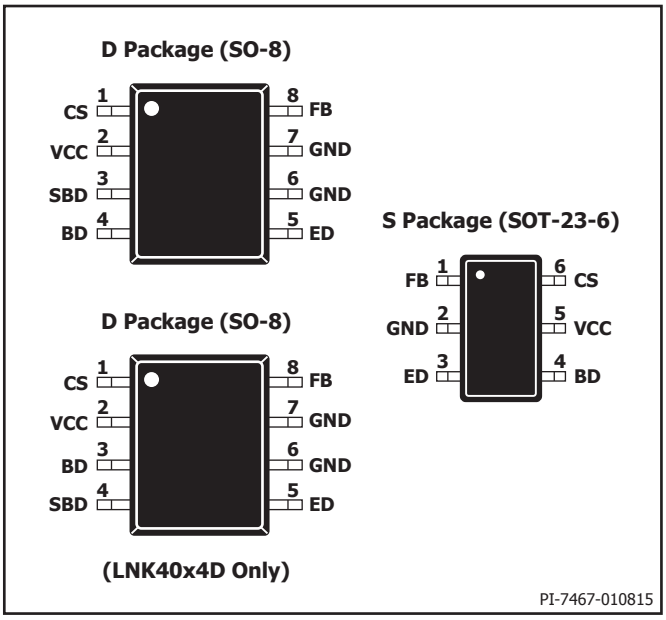


Figure 6. Pin Configuration.

Functional Description

Power-Up/Power-Down Sequences

Refer to Figure 10 and Figure 7. When mains input voltage (V_{IN}) is applied, current flows through the start-up resistors (R_{HT}) and BJT. Some of this current flows into the LinkSwitch-4 internal circuits, which are in Sleep mode; the remainder charges capacitor C_{VCC}. As soon as the VOLTAGE SUPPLY pin voltage rises to $V_{VCC(RUN)}$, the LinkSwitch-4 changes to Initialise mode. Current consumption increases to $I_{VCC(RUN)}$ while internal circuits are enabled. The emitter switch is held at low impedance to ground (GND) and a short drive pulse is output on the BASE DRIVE pin, during which time the voltage at feedback is held at GND potential by current sourced from the FEEDBACK pin. This enables the LinkSwitch-4 control circuit to compare the rectified mains input voltage with thresholds for allowing or preventing the next stage of power-up. If the input voltage is too low ($I_{FB} < I_{FBHT(START)}$), the LinkSwitch-4 will not issue further drive pulses, the VCC voltage will discharge to $V_{VCC(SLEEP)}$, and the power-up sequence will repeat. If the mains input voltage is high enough ($I_{FB} > I_{FBHT(START)}$), the LinkSwitch-4 will enter Run mode and drive pulses will be output on the BASE DRIVE pin. To achieve smooth power-up (monotonic rise in V_{OUT}), C_{VCC} must be large enough to power the control circuitry during Initialize mode and the first few cycles of Run mode, until sufficient power is provided by the transformer voltage supply winding.

If the input voltage falls below $V_{MAINS(LO)}$ (see Input Undervoltage Protection), V_{VCC} will fall below $V_{VCC(SLEEP)}$ and the LinkSwitch-4 will go into Sleep mode, reducing its current consumption to $I_{VCC(SLEEP)}$. The control circuitry will re-initialize if the input voltage is restored and V_{VCC} reaches $V_{VCC(RUN)}$.

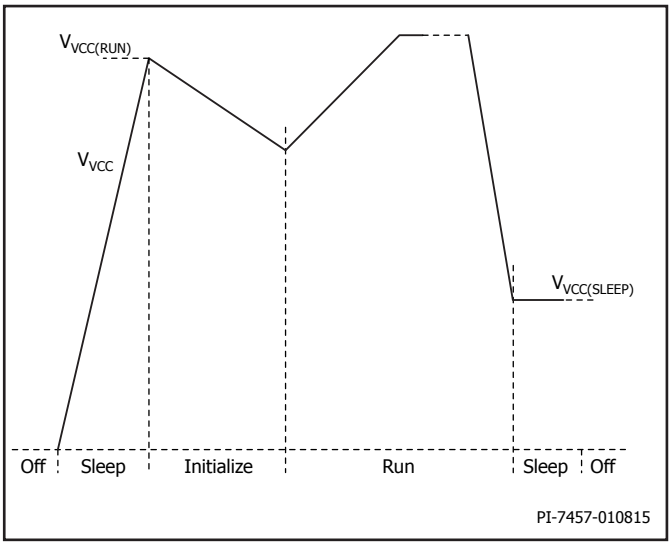


Figure 7. VCC Waveforms.

Mode	Description
Sleep	From initial application of input power or from Run mode, if V_{VCC} falls below $V_{VCC(SLEEP)}$, the LinkSwitch-4 goes to Sleep mode. Non-essential circuits are turned off and base drive is held low. Sleep mode is exited when V_{VCC} rises to $V_{VCC(RUN)}$ and the control circuitry goes to Initialize mode.
Initialize	Internal circuits are enabled and the LinkSwitch-4 issues one switching cycle to sample the input voltage via the FEEDBACK pin. If V_{IN} (hence V_{HT}) is high enough, the LinkSwitch-4 changes to Run mode. If V_{IN} is not high enough, no further base drive pulses are issued and the LinkSwitch-4 returns to Sleep mode when V_{VCC} falls below $V_{VCC(SLEEP)}$.
Run	Power conversion: The control circuitry is powered from the VCC rail and the internal V_{DD} is regulated. If V_{VCC} falls below $V_{VCC(SLEEP)}$, the IC ceases power conversion and goes to Sleep mode.

Table 2. Summary of LinkSwitch-4 Operating Modes.

Switching Waveforms

Typical waveforms at the feedback and primary current sense inputs are shown in Figure 8.

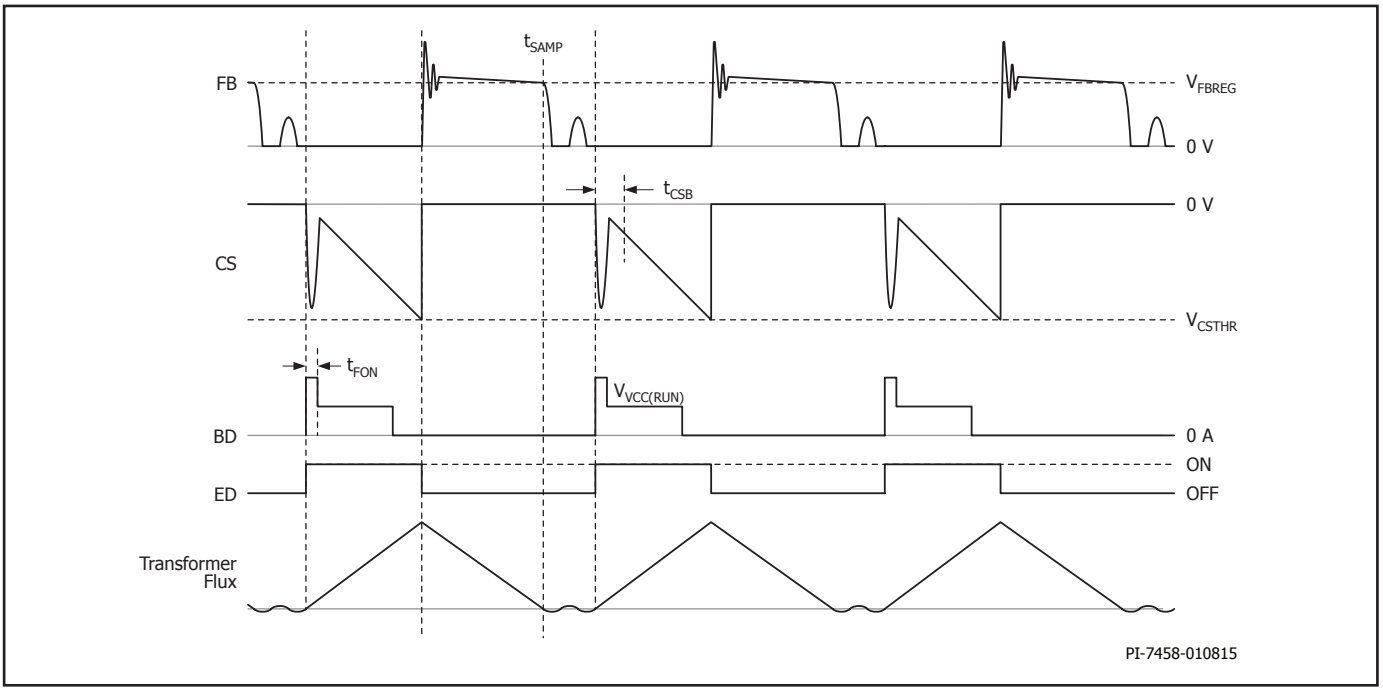


Figure 8. Typical Waveforms at the Feedback and Primary Current Sense Inputs.

Constant Voltage (CV) Regulation

Constant output voltage regulation is achieved by sensing the voltage at the feedback input, which is connected to the voltage supply winding as shown in Figure 10 or to a dedicated feedback winding. An internal current source prevents the feedback voltage from going negative. A typical feedback voltage waveform is shown in Figure 8. The feedback waveform is continuously analyzed and sampled at time t_{SAMP} to measure the reflected output voltage. t_{SAMP} is identified by the slope of the feedback waveform and is coincident with zero flux in the transformer. The sampled voltage is regulated at $V_{FB(REG)}$ by the voltage control loop. The (typical) CV mode output voltage is set by the ratio of resistors R_{FB1} and R_{FB2} (see Figure 10) and by the transformer turns ratio, according to the following formula (where output diode voltage is neglected):

$$V_{OUT(CV)} = V_{FB(REG)}\left(1+\frac{R_{FB1}}{R_{FB2}}\right)\left(\frac{N_S}{N_F}\right)$$

Where N_F is the number of turns on the feedback (or voltage supply if used for feedback) winding and N_S is the number of turns on the secondary winding. The tolerances of R_{FB1} and R_{FB2} affect output voltage regulation and mains estimation so should typically be chosen to be 1% or better.

The current required to clamp the feedback voltage to ground potential during the on-time of the primary switch depends on the primary winding voltage (approximately equal to the rectified mains input voltage), the primary to feedback turns ratio, and resistor R_{FB1}. The controller measures feedback source current and so enables R_{FB1} to set the input voltage start threshold and the input undervoltage protection threshold, as described below.

Input Voltage Start Threshold

In Initialise mode, the LinkSwitch-4 issues a single short-duration drive pulse in order to measure the primary voltage and so the approximate mains input voltage. If the input voltage is below $V_{MAINS(START)}$ then the LinkSwitch-4 will not start. Instead it will pause while V_{VCC} discharges below $V_{VCC(SLEEP)}$ then it will begin a new power-up cycle. If the input voltage exceeds $V_{MAINS(START)}$, the converter will power-up. $V_{MAINS(START)}$ is set by R_{FB1} using this equation:

$$V_{MAINS(START)} = \frac{-1}{\sqrt{2}} \times I_{FBHT(START)} \times R_{FB1} \times \frac{N_P}{N_F}$$

Input Undervoltage Protection

In Run mode, if the mains voltage falls to $V_{MAINS(LO)}$, the LinkSwitch-4 will stop issuing drive pulses, V_{VCC} will reduce to $V_{VCC(SLEEP)}$ and the LinkSwitch-4 will enter Sleep mode. $V_{MAINS(LO)}$ is set by R_{FB1} using this equation:

$$V_{MAINS(LO)} = \frac{-1}{\sqrt{2}} \times I_{FBHT(LO)} \times R_{FB1} \times \frac{N_P}{N_F}$$

Constant Current (CC Mode) Regulation

Constant current output ($I_{OUT(CC)}$) is achieved by regulating the CS input to the primary side estimate of the output current scaled by R_{CS}, $V_{CS(CC)}$. The regulated output current, $I_{OUT(CC)}$ is set by the value of the current sense resistor, R_{CS}, and the transformer primary to secondary turns ratio (N_P/N_S). The value of R_{CS} is determined using the formula:

$$R_{CS} \approx \left(\frac{N_P}{N_S}\right)\left(\frac{V_{CS(CC)}(Typ)}{I_{OUT(CC)}(Typ)}\right)$$

The tolerance of R_{CS} affects the accuracy of output the current regulation so is typically chosen to be 1%. The LinkSwitch-4 can maintain CC regulation down to much lower levels of $V_{SHUTDN(MAX)}$ normally specified for mobile phones chargers (see Figure 11).

Cable Compensation

If required, LinkSwitch-4 adjusts the converter output voltage (V_{OUT}) to compensate for voltage drop across the output cable. The amount of compensation applied (G_{CAB}) is specified by using the formula below to match cable compensation with output cable resistance (R_{CAB}).

$$G_{CAB} = \frac{I_{OUT(CC)}(Typ) \times R_{CAB}}{V_{OUT(CV)}(Typ)} \times 100\%$$

Drive Pulse and Frequency Modulation

The LinkSwitch-4 control circuitry determines both the primary switch peak current and the switching frequency to control output power, ensuring discontinuous conduction mode operation at all times.

Primary current generates a voltage across the current sense resistor, R_{CS}, and is sensed by the primary current sense input. The voltage on the primary CURRENT SENSE pin is negative-going, as shown in Figure 8. When the voltage exceeds a (negative) threshold (V_{CSTHR}) set by the control circuitry, base drive is driven low to turn the primary switch off. The primary current sense voltage threshold (V_{CSTHR}) varies from $V_{CS(MIN)}$ to $V_{CS(MAX)}$ during normal operation. The switching frequency varies from f_{MIN} at no-load, to the maximum switching frequency, f_{MAX}.

Minimum switching frequency occurs during no-load operation and is typically in the range 1 to 3 kHz, depending on application design. The periodic voltage waveform on the VCC input, which depends on the current consumed by the control circuitry and the value of C_{VCC}, contributes to control of the switching frequency. In no-load condition, C_{VCC} must be large enough to ensure that ripple voltage on VCC is less than $\Delta V_{VCCPFM(MAX)}$, and C_{VCC} must be small enough to ensure the ripple on VCC is greater than $\Delta V_{VCCPFM(MIN)}$.

$$C_{VCC} = \frac{I_{VCCNL}}{f_{MIN} \times \Delta V_{VCCPFM}}$$

The switching frequency increases as the load increases, eventually reaching f_{MAX} at full load. For protection purposes in the event of certain transitory conditions, the controller immediately issues a drive pulse if VCC voltage falls to $V_{VCC(LOW)}$. This is not part of normal operation or normal frequency control.

Base Drive Control

During the on-time of the BJT, the emitter is switched to GND via the EMITTER DRIVE pin. Base current, I_{BD} is controlled to achieve fast turn-on, low on-voltage and fast turn-off to enable reduced power dissipation and accurate timing of each part of the switching cycle.

As shown in Figure 9, the base drive current starts with a fixed pulse of $I_{F(ON)}/t_{F(ON)}$. Its amplitude and duration are then modulated to provide sufficient charge for low BJT on-voltage, while allowing de-saturation towards the end of on-time so as to enable fast turn-off. When V_{CSTHR} is detected on the primary CURRENT SENSE pin, the BASE DRIVE pin is switched to GND and the emitter drive switch is opened.

Duty Cycle Control

Maximum duty cycle is a function of the primary to secondary turns ratio of the transformer (typically 16:1 for a 5 V output). For a universal mains input power supply, maximum duty cycle is typically chosen to be 50% at the minimum (including ripple) of the rectified mains voltage (typically 80 V).

Quasi-Resonant Switching

The primary switch is turned on when the voltage across it rings down to a minimum (voltage-valley, quasi-resonant switching). The effect of this is to reduce losses in the switch at turn-on. It also helps reduce EMI.

Primary Switch Over-Current Protection

The primary switch is turned off if the emitter current sensed by the primary current sense input exceeds the effective threshold $V_{CSOCP(EFF)}$, subject to the minimum on-time, $T_{ON(MIN)}$. The effective threshold $V_{CSOCP(EFF)}$ depends on a threshold $V_{CS(OCP)}$ predefined by the controller, the primary current sense signal rate of rise (dVcs/dt), which is dependent on the application design, and the primary CURRENT SENSE pin turn-off response time, $t_{CS(OFF)}$. This gives pulse by pulse over-current protection of the primary switch.

Output Overvoltage Protection

The on-time of the primary switch is reduced if the output voltage tends to $V_{OUT(OVP)}$. The value depends on the set output voltage ($V_{OUT(CV)}$) and the feedback OVP ratio:

$$V_{OUT(OVP)} = V_{OUT(CV)} \times G_{FB(OVP)}$$

Supplementary Base Drive

The resistor R_{SBD} connects the SUPPLEMENTARY BASE DRIVE pin to VOLTAGE SUPPLY pin. It supplements current to the base drive to optimize the switching bipolar transistor turn-on and turn-off in high power applications.

Suggested values for the supplementary base drive resistor R_{SBD} are between 220 Ω and 390 Ω.

Shunt Function

The shunt function is intended to automatically limit the VCC voltage and allow greater flexibility in transformer design. VOLTAGE SUPPLY pin will be shunted via R_{SBD}, the SUPPLEMENTARY BASE DRIVE pin resistance $R_{SBD(ON)}$ and $R_{BD(OFF)}$ to the GROUND pin when the VCC voltage is greater than $V_{VCC(HI)}$ and the transformer is discharging.

Output Undervoltage Protection (LNK40x3D/S Only)

The output undervoltage protection (UVP) function is used to shutdown the converter when the output voltage is below $V_{OUT(UVP)}$.

At start-up this function is disabled during the first $N_{STARTUP}$ switching cycles and the output current is regulated allowing the output voltage to rise from 0 V in a monotonic way.

If the output does not reach $V_{OUT(UVP)}$ during this time then the controller will shutdown and restart.

$V_{OUT(UVP)}$ value depends on the set output voltage ($V_{OUT(CV)}$) and the feedback UVP ratio:

$$V_{OUT(UVP)} = V_{OUT(CV)} \times G_{FB(UVP)}$$

Product	Output Undervoltage Protection Function
LNK40x2S	$V_{OUT(UVP)}$ Depends on $V_{VCC(SLEEP)}$
LNK40x3S LNK40x3D	$V_{OUT(UVP)} = 0.6 \times V_{OUT(CV)}$
LNK40x4D	$V_{OUT(UVP)}$ Depends on $V_{VCC(SLEEP)}$

Table 3. Output Undervoltage Protection.

Over-Temperature Protection

Temperature protection is internal to LinkSwitch-4. The sensor measures the junction temperature T_J, which is the hottest part of LinkSwitch-4.

At temperatures T_J ~ 140 °C, LinkSwitch-4 will shutdown and remain in this state until a temperature of T_J ~ 70 °C is reached. Whereby LinkSwitch-4 will power-up in the normal sequence.

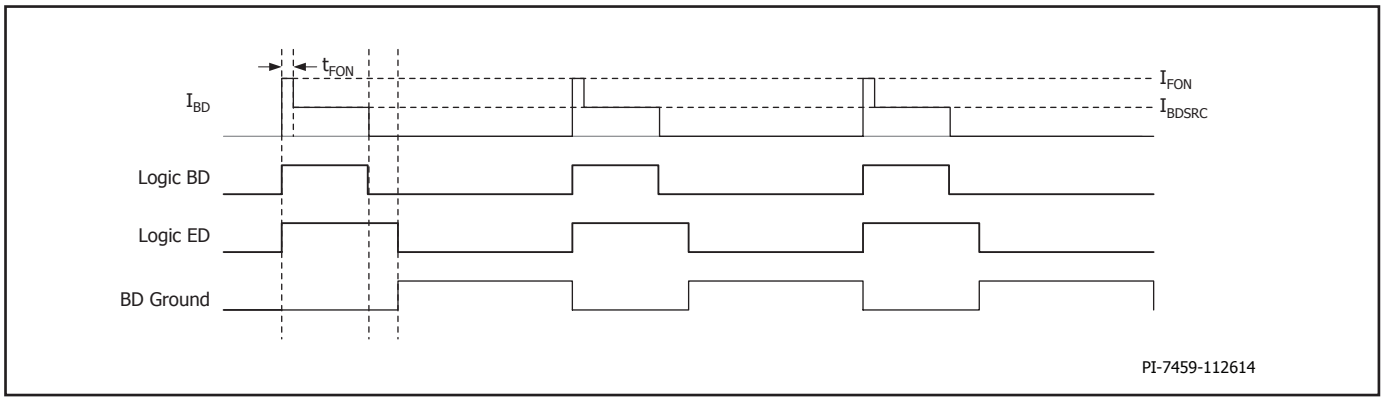


Figure 9. Base Drive Waveforms.

Typical Application

Parameter	Symbol	Range or Value	Units	Comment
Supply Voltage	V_{IN}	85 - 265	VAC	Universal mains
Output Voltage	$V_{OUT(CV)}$	5.0 ± 5%	V	Constant voltage (CV) mode, at the load
Output Current	$I_{OUT(CC)}$	2	A	Constant current (CC) mode
Switching Frequency at Full Load	f_{MAX}	65	kHz	Determined by the chosen variant
Cable Compensation	G_{CAB}	6	%	Determined by the chosen variant
No-load Power	P_{NL}	<30	mW	Energy Star test method
Average Efficiency	η	>75	%	Energy Star test method
Turn-on Delay	T_{ON}	<1	s	
Undershoot Voltage	$V_{UNDERSHT}$	>4	V	Load step from 0 A to 0.5 A

Table 4. 10 W Typical Application Results for Figure 10.

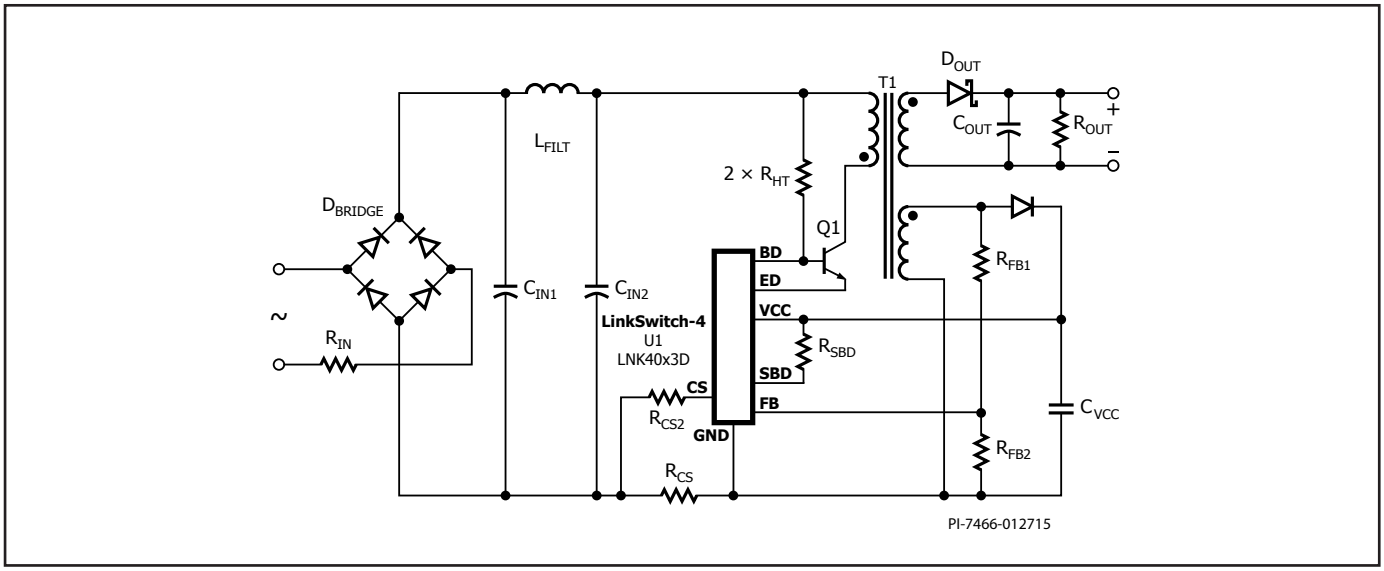


Figure 10. Typical Universal Input, 10 W Charger.

By sensing the primary-side waveforms of transformer voltage and primary current, the LinkSwitch-4 achieves constant voltage and constant current output within tight limits without the need for any secondary-side sensing components. Figure 11 shows the output characteristics of a typical charger implementation.

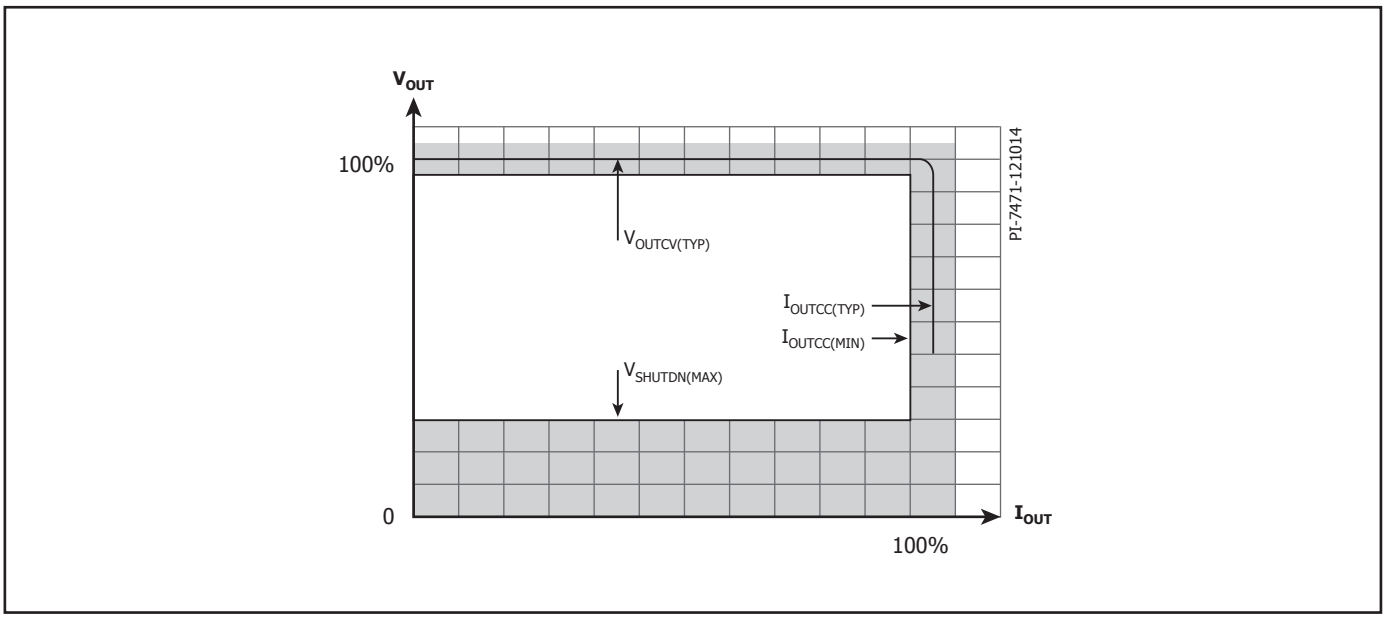


Figure 11. Typical CV/CC Output Characteristic Achieved.

Absolute Maximum Ratings[2]

SUPPLY VOLTAGE Pin .....-0.5 V to 18 V
FEEDBACK Pin Input Voltage ..... -0.5 V to 4 V
FEEDBACK Pin Input Current ..... -20 mA to 20 mA
CURRENT SENSE Pin Input Voltage..... -0.5 V to 4 V
CURRENT SENSE Pin Input Current..... -20 mA to 20 mA
BASE DRIVE Pin Voltage.....-0.5 V to 18 V
EMITTER DRIVE Pin Voltage.....-0.5 V to 18 V
SUPPLEMENTARY BASE DRIVE Pin Voltage.....-0.5 V to 18 V
Junction Temperature ..... -40 to 125 °C
Lead Temperature[1].....260 °C

Notes:
1. Soldering, 10 seconds.
2. Maximum ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum ratings for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: D Package: (SO-8)
(θ_{JA}) ..... 120 °C/W
(θ_{JB})[1,2] .....30 °C/W
S Package (SOT-23-6)
(θ_{JA}) ..... 170 °C/W
(θ_{JB})[2] .....60 °C/W

Notes:
1. IC mounted on typical (1oz) copper clad PCB with 164 mm^2 ground plane surrounding GROUND pin(s).
2. θ_{JB} measured to GROUND pin terminal of device at the surface of the PCB.

Parameter	Symbol	Conditions T_J = -25 to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Normal Operating Conditions						
External Supply Voltage	V_{VCC}		5		16.5	V
Transformer Resonance frequency (In-Circuit)	f_{RES}		180		1200	kHz
Thermal Shutdown Temperature	T_{SD}		130	140	150	°C
Thermal Shutdown Hysteresis	T_{SDH}			70		°C
VOLTAGE SUPPLY Pin						
Supply Voltage	$V_{VCC(RUN)}$	To Enter Initialize Mode	11.5	13.5	15.5	V
	$V_{VCC(SLEEP)}$			4.5		
	$V_{VCC(LOW)}$			5		
Supply Current	$I_{VCC(RUN)}$	Average at f_{MAX}, Excluding Base Drive Current		2		mA
	$I_{VCC(NL)}$	No-Load		0.6		
	$I_{VCC(SLEEP)}$	In Sleep Mode			15	µA
VCC Voltage Peak-to-Peak Amplitude	$\Delta V_{VCC(PFM)}$	No-Load	0.05		1.6	V
FEEDBACK Pin						
Feedback Regulation Level	$V_{FB(REG)}$	T_J = 25 °C	1.96	1.98	2.00	V
Feedback Input Resistance	$R_{FB(IN)}$	Effective Input Resistance 0 < V_{FB} < 5		2		MΩ

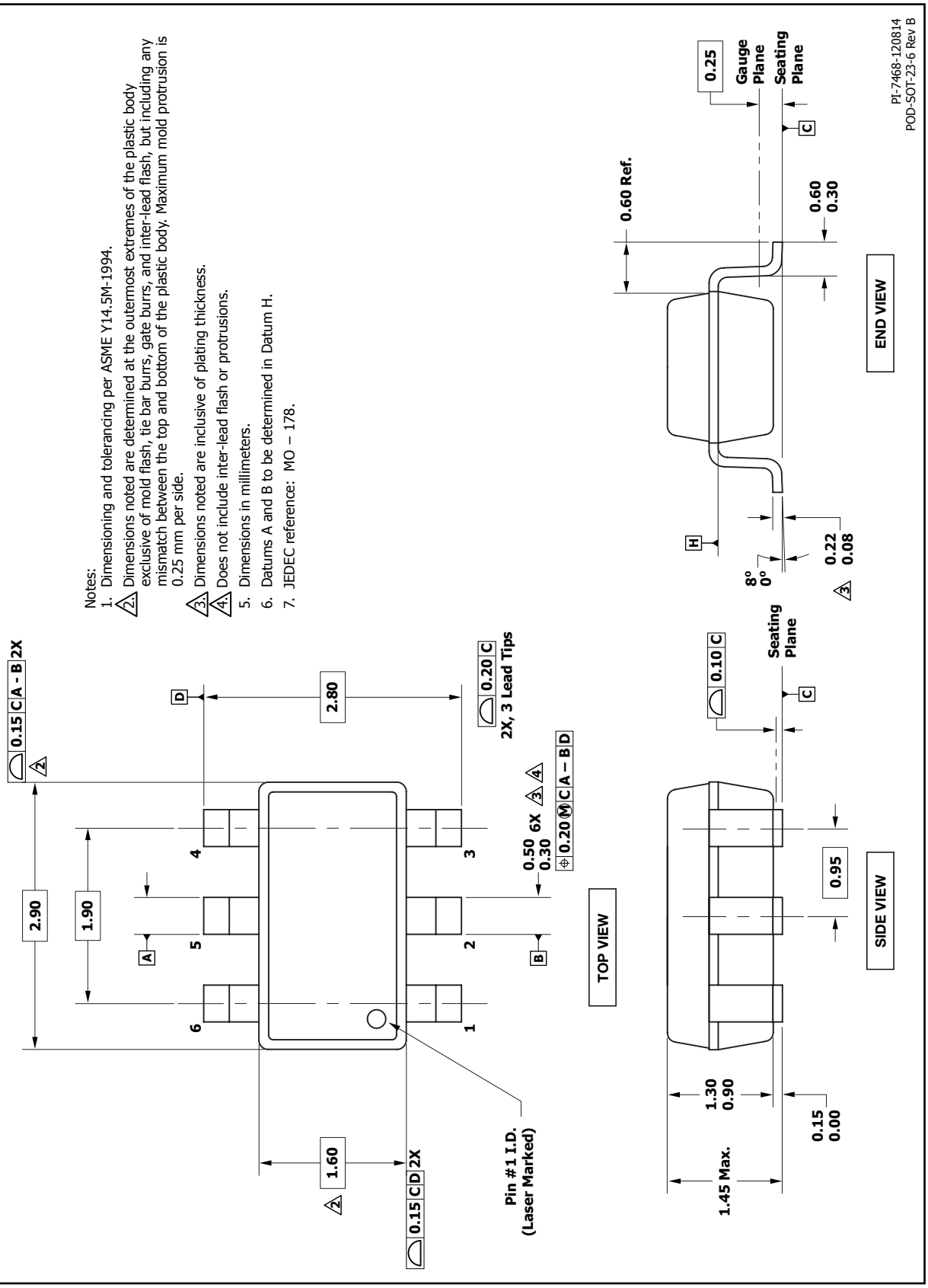
Parameter	Symbol	Conditions T_J = -25 to 125 °C (Unless Otherwise Specified)			Min	Typ	Max	Units
FEEDBACK Pin (Cont.)								
Feedback OVP Ratio	$G_{FB(OVP)}$					1.20		
Feedback UVP Ratio	$G_{FB(UVP)}$	LNK40x3D/S Only				0.6		
Feedback Current Low Mains Threshold	$I_{FBHT(LO)}$					-0.45		mA
Feedback Current Start Mains Threshold	$I_{FBHT(START)}$				-1.05			mA
Feedback Blanking Time	$T_{FB(BL)}$	LNK40x2S				1.5		µs
		$\frac{V_{OUT}}{V_{OUT(CV)}}$ ≤0.7	R_{CS2} = 100 Ω			1.5		
			R_{CS2} = 270 Ω			2.2		
			R_{CS2} = 470 Ω			2.5		
			R_{CS2} = 1000 Ω			2.5		
		$\frac{V_{OUT}}{V_{OUT(CV)}}$ >0.7	R_{CS2} = 100 Ω			0.75		
			R_{CS2} = 270 Ω			1.1		
			R_{CS2} = 470 Ω			1.25		
			R_{CS2} = 1000 Ω			1.25		
Start-up Cycle Count	$N_{STARTUP}$	LNK40x3S / LNK40x3D				600		
Transient Detect Pulse Duration	T_{TD}	LNK40x3S / LNK40x3D / LNK40x4D				100		ns
Transient Detect Threshold	V_{TD}	LNK40x3S / LNK40x3D / LNK40x4D				60		mV
CURRENT SENSE Pin								
Primary Current Sense Input Minimum Threshold	$V_{CS(MIN)}$	Outside Primary Current Sense Blanking Time $t_{CS(B)}$	LNK40x2S			-88		mV
			LNK40x3S / LNK40x3D / LNK40x4D (Set by External Resistor R_{CS2})	R_{CS2}= 100 Ω		-56		
				R_{CS2}= 270 Ω		-73		
				R_{CS2}= 470 Ω		-94		
				R_{CS2}= 1000 Ω		-127		
Primary Current Sense Input Maximum Threshold	$V_{CS(OCP)}$	Outside Primary Current Sense Blanking Time $t_{CS(B)}$	Over-Current Protect		-350	-340	-330	mV
	$V_{CS(MAX)}$		Normal Regulation		-380	-360	-340	mV
Primary Current Sense Turn-Off Response Time	$t_{CS(OFF)}$	Outside Primary Current Sense Blanking Time $t_{CS(B)}$				120		ns
Primary Current Sense Threshold for CC Operation	$V_{CS(CC)}$	T_J = 25 °C			-62	-60.8	-59.6	mV
Leading Edge Blanking Time	$t_{CS(B)}$	See Figure 8				375		ns

Parameter	Symbol	Conditions T_J = -25 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
BASE DRIVE Pin							
Base Drive Force on Current	$I_{F(ON)}$	LNK40x2S / LNK40x3S / LNK40x3D			40		mA
		LNK40x4D			80		
Base Drive Force on Duration	$T_{F(ON)}$				200		ns
Base Drive Source Current	$I_{BDSRC(MIN)}$	LNK40x2S / LNK40x3S / LNK40x3D			5		mA
		LNK40x4D			12		
	$I_{BDSRC(MAX)}$	LNK40x2S / LNK40x3S / LNK40x3D			40		
		LNK40x4D			80		
Base Drive Pull Down Resistance	$R_{BD(OFF)}$	V_{VCC} = 12 V	LNK40x2S		4.5		Ω
			LNK40x3S		3		
			LNK40x3D		3		
			LNK40x4D		1.2		
Base Drive Minimum On-Time	$t_{BDON(MIN)}$				375		ns
Base Drive Leakage Current	$I_{BD(SLEEP)}$	In Sleep Mode, T_J = 50 °C				1	µA
Base Drive Peak Sink Current	$I_{BD(SINK)}$	LNK40x2S				600	mA
		LNK40x3S				700	
		LNK40x3D				900	
		LNK40x4D				1100	
EMITTER DRIVE Pin							
Emitter Drive On-State Resistance	$R_{EDON(MAX)}$	V_{VCC} = $V_{VCC(SLEEP)}$	LNK40x2S		3		Ω
			LNK40x3S		1.5		
			LNK40x3D		1.5		
			LNK40x4D		0.9		
Emitter Drive Leakage Current	$I_{ED(SLEEP)}$	In Sleep Mode, T_J = 50 °C	LNK40x2S			1	µA
			LNK40x3S			1	
			LNK40x3D			1	
			LNK40x4D			1	
Emitter Drive Peak Sink Current	$I_{ED(SINK)}$	LNK40x2S				600	mA
		LNK40x3S				700	
		LNK40x3D				900	
		LNK40x4D				1100	
Emitter Drive Minimum On-Time	$t_{EDMIN(ON)}$	LNK40x3S / LNK40x3D Only			175		ns

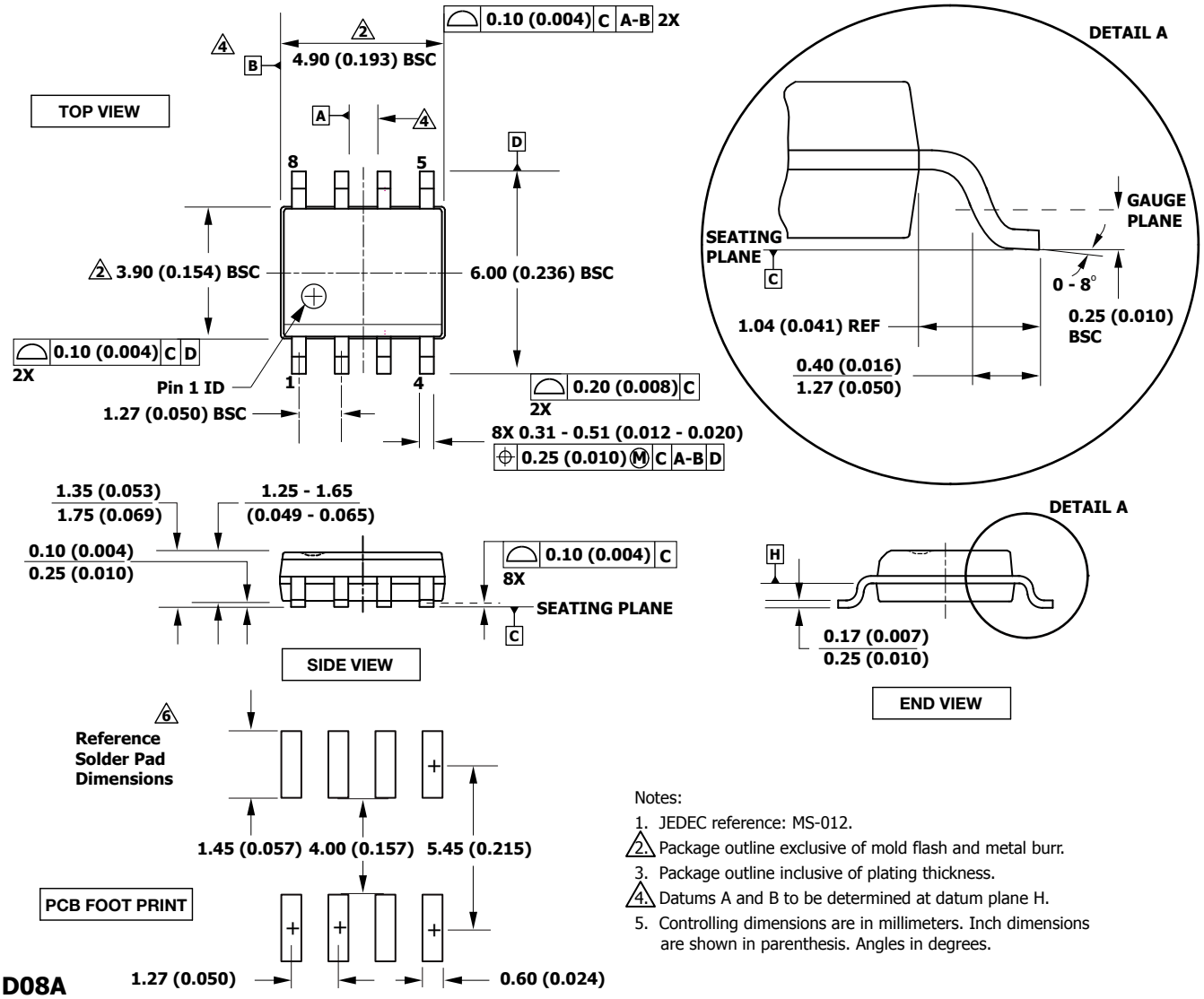
Parameter	Symbol	Conditions T_J = -25 to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
SBD Pin							
SBD On-State Resistance	$R_{SBD(ON)}$		LNK40x3D / LNK40x4D		8		Ω
SBD Leakage Current	$I_{SBD(SLEEP)}$	In Sleep Mode, T_J = 50 °C	LNK40x3D / LNK40x4D			1	µA

NOTES:
A. Min and Max values apply over the full range of normal operating conditions.
B. Typical electrical characteristics apply at $T_J = T_J$ (typ).
C. The chip is operating in Run mode.
D. Voltages are specified with respect to the GROUND pin.

SOT-23-6


Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.25 mm per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Dimensions in millimeters.
6. Datums A and B to be determined in Datum H.
7. JEDEC reference: MO – 178.
TOP VIEW
SIDE VIEW
END VIEW
Pin #1 I.D. (Laser Marked)
Seating Plane
Gauge Plane
2X, 3 Lead Tips
PI-7468-120814
POD-SOT-23-6 Rev B

SO-8 (D Package)



D08A

Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

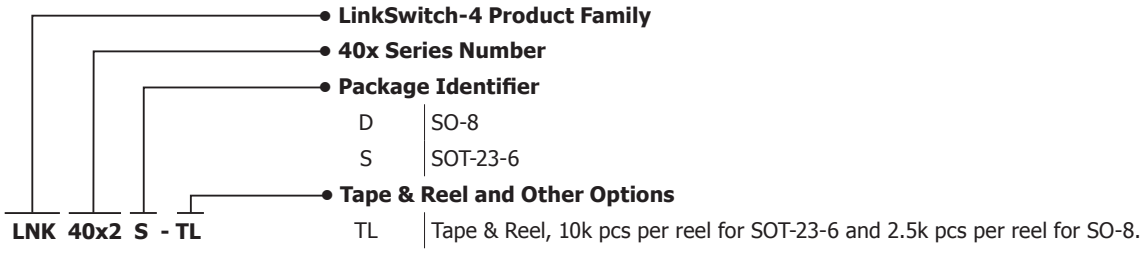
PI-7461-120914

Part Ordering Table

Product	f_{MAX} (kHz)	G_{CAB} (%)	Package Marking[1]	Tape and Reel Part Number
LNK4002S	65	0	BBxx	LNK4002S-TL
LNK4012S	65	3	GBxx	LNK4012S-TL
LNK4022S	65	6	BAxx	LNK4022S-TL
LNK4003S	65	0	DLxx	LNK4003S-TL
LNK4013S	65	3	DOxx	LNK4013S-TL
LNK4023S	65	6	DNxx	LNK4023S-TL
LNK4003D	65	0	LNK4003D	LNK4003D-TL
LNK4013D	65	3	LNK4013D	LNK4013D-TL
LNK4023D	65	6	LNK4023D	LNK4023D-TL
LNK4004D	65	0	LNK4004D	LNK4004D-TL
LNK4014D	65	3	LNK4014D	LNK4014D-TL
LNK4024D	65	6	LNK4024D	LNK4024D-TL

NOTES:
1. xx = Manufacturing lot code.

Part Ordering Information



Revision	Notes	Date
A	Initial Release.	01/27/15
B	Added Over-Temperature Protection section. Added LNK4012S, LNK4013S and LNK4013D parts.	04/06/15

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