2 × 2 W, Filterless, Stereo, Class-D Audio Amplifier with ALC and I²C

SSM2380

FEATURES

Filterless, stereo, Class-D amplifier with Σ-Δ modulation
2 W into 4 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with <1% total harmonic distortion plus noise (THD + N)
Highly configurable I²C interface for gain adjust, automatic level control (ALC), and ultralow EMI emissions mode
MODE pin can disable I²C interface for more traditional stereo amplifier configuration
Stereo-to-mono mixer option via I²C control
93% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Signal-to-noise ratio (SNR): >100 dB
Single-supply operation from 2.5 V to 5.5 V
Ultralow shutdown current: 20 nA
Short-circuit and thermal protection
Pop-and-click suppression
Available in 16-ball, 2.0 mm × 2.0 mm WLCSP

APPLICATIONS

Mobile phones
MP3 players
Portable electronics

GENERAL DESCRIPTION

The SSM2380 is a fully integrated, high efficiency, stereo, Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 2 W of continuous output power with <1% THD + N driving a 4 Ω load from a 5.0 V supply.

The SSM2380 features a highly flexible I²C interface with many useful settings. Using the I²C control interface, the gain of the SSM2380 can be selected from 1 dB to 24 dB (plus mute) in 47 steps with no external components. Other features accessed from the I²C interface include independent left/right channel shutdown, variable ultralow EMI emission control mode, automatic level control (ALC) for high quality speaker protection, and stereo-to-mono mixing operation.

The SSM2380 features a high efficiency, low noise modulation scheme that requires no external LC output filters. The modulation continues to provide high efficiency even at low output power. The SSM2380 operates with 93% efficiency at 1.4 W into 8 Ω or with 85% efficiency at 2 W into 4 Ω from a 5.0 V supply and has an SNR of >100 dB.

Spread-spectrum pulse density modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures. An added benefit of spread-spectrum Σ-Δ modulation is that no synchronization (SYNC) is needed when using multiple Class-D amplifiers. For applications that require long speaker cables (>10 cm), the SSM2380 includes a user-selectable ultralow EMI emissions mode that eliminates the need for EMI filters at the Class-D outputs.

The SSM2380 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin or through an optional independent channel soft shutdown via I²C.

The device also includes pop-and-click suppression circuitry. This suppression circuitry minimizes voltage glitches at the output during turn-on and turn-off, reducing audible noise on activation and deactivation.

The fully differential inputs of the SSM2380 provide excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The SSM2380 is specified over the commercial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 16-ball, 2 mm × 2 mm wafer level chip scale package (WLCSP).

Rev. A
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REVISION HISTORY

2/11—Rev. 0 to Rev. A

Changes to Setting the ALC Threshold Voltage Section ... 15

10/10—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

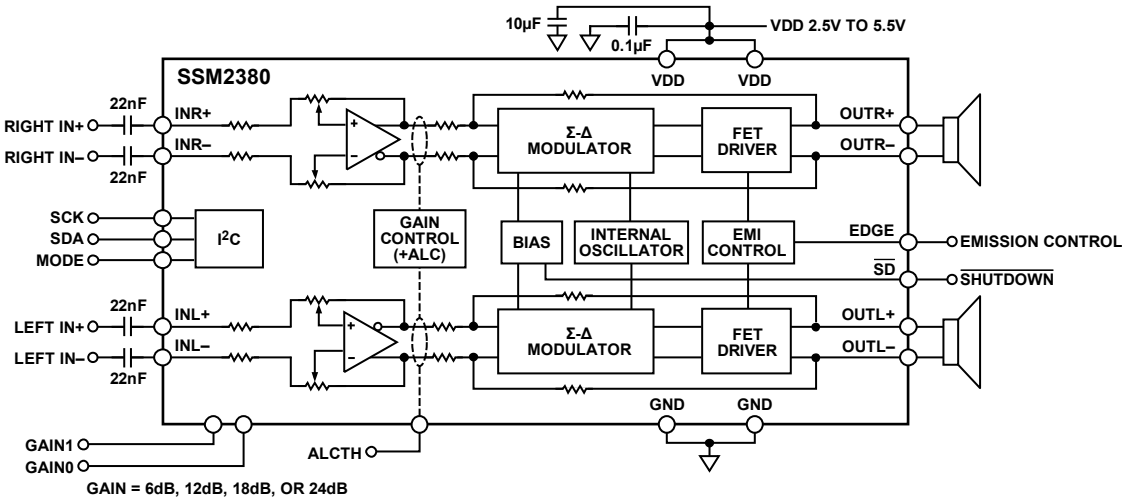

Figure 1.

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω +33 µH, gain = 6 dB, I^2C control mode, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments[1]	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS		f = 1 kHz, 20 kHz bandwidth				
Output Power	P_O	R_L = 8 Ω, THD = 1%, V_{DD} = 5.0 V		1.43		W
		R_L = 8 Ω, THD = 1%, V_{DD} = 3.6 V		0.73		W
		R_L = 8 Ω, THD = 10%, V_{DD} = 5.0 V		1.8		W
		R_L = 8 Ω, THD = 10%, V_{DD} = 3.6 V		0.92		W
		R_L = 4 Ω, THD = 1%, V_{DD} = 5.0 V		2.58[1]		W
		R_L = 4 Ω, THD = 1%, V_{DD} = 3.6 V		1.3		W
		R_L = 4 Ω, THD = 10%, V_{DD} = 5.0 V		3.2[1]		W
		R_L = 4 Ω, THD = 10%, V_{DD} = 3.6 V		1.62		W
Efficiency	η	P_O = 1.4 W into 8 Ω, V_{DD} = 5.0 V				
		Normal, low EMI mode		93		%
		Ultralow EMI mode		91		%
Total Harmonic Distortion Plus Noise	THD + N	P_O = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.005		%
		P_O = 0.5 W into 8 Ω, f = 1 kHz, V_{DD} = 3.6 V		0.005		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1.0	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, output referred		55		dB
Channel Separation	X_{TALK}	P_O = 100 mW, f = 1 kHz		78		dB
Average Switching Frequency	f_{SW}			325		kHz
Differential Output Offset Voltage	V_{OOS}	Gain = 6 dB		2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac-grounded, C_{IN} = 0.1 µF		60		dB
Supply Current, Stereo	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		6.8		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		6.0		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		5.8		mA
		V_{IN} = 0 V, R_L = 8 Ω + 33 µH, V_{DD} = 5.0 V		7.0		mA
		V_{IN} = 0 V, R_L = 8 Ω + 33 µH, V_{DD} = 3.6 V		6.1		mA
		V_{IN} = 0 V, R_L = 8 Ω + 33 µH, V_{DD} = 2.5 V		5.5		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Gain	GAINx = I^2C control mode	1		24	dB
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}		1.35			V
Input Voltage Low	V_{IL}				0.35	V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to VDD		7		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from VDD to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac-grounded, gain = 6 dB, A-weighted		30		µV rms
Signal-to-Noise Ratio	SNR	P_O = 1.4 W, R_L = 8 Ω, gain = 6 dB		100		dB
		P_O = 1.4 W, R_L = 8 Ω, gain = 24 dB		90		dB

[1] Although the SSM2380 has good quality above 2 W, continuous output power beyond 2 W must be avoided due to device packaging limitations.

I²C TIMING CHARACTERISTICS

Table 2.

Parameter	Limit		Unit	Description
	t_{MIN}	t_{MAX}		
t_{SCS}	600		ns	Start condition setup time
t_{SCH}	600		ns	Start condition hold time
t_{PH}	600		ns	SCK pulse width high
t_{PL}	1.3		µs	SCK pulse width low
f_{SCK}	0	526	kHz	SCK frequency
t_{DS}	100		ns	Data setup time
t_{DH}		900	ns	Data hold time
t_{RT}		300	ns	SDA and SCK rise time
t_{FT}		300	ns	SDA and SCK fall time
t_{HCS}	600		ns	Stop condition setup time

Timing Diagram

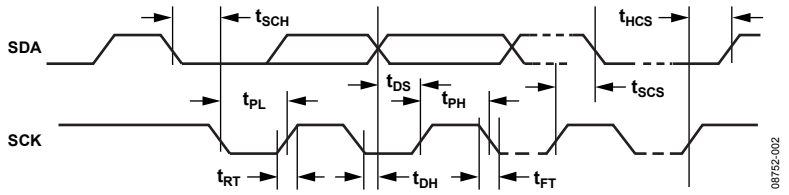

Figure 2. I²C Timing

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
16-Lead, 2.0 mm × 2.0 mm WLCSP	2S2P	57	14	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

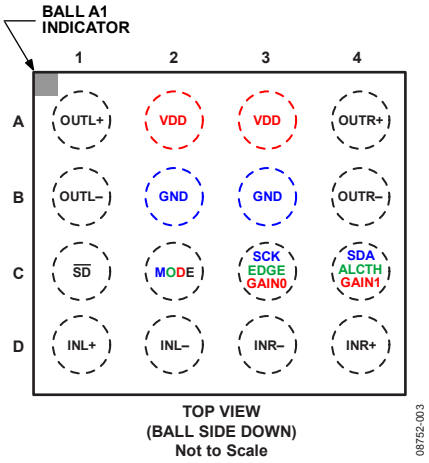

Figure 3. Pin Configuration (Bottom View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	OUTL+	Noninverting Output for Left Channel.
A2, A3	VDD	Power Supply for Output Amplifiers.
A4	OUTR+	Noninverting Output for Right Channel.
B1	OUTL–	Inverting Output for Left Channel.
B2, B3	GND	Ground for Output Amplifiers.
B4	OUTR–	Inverting Output for Right Channel.
C1	$\overline{SD}$	Shutdown Input. Active low digital input.
C2	MODE	Three-Mode Interface Control Pin.
C3	SCK/EDGE/GAIN0	2-Wire I^2C Control Interface Clock Input (SCK). MODE is connected to GND. Low Emissions Mode Enable Pin (EDGE). MODE is floating. Gain Select Pin, LSB (GAIN0). MODE is connected to VDD.
C4	SDA/ALCTH/GAIN1	2-Wire I^2C Control Interface Data Input/Output (SDA). MODE is connected to GND. Variable Threshold Voltage for ALC (ALCTH). MODE is floating. Gain Select Pin, MSB (GAIN1). MODE is connected to VDD.
D1	INL+	Noninverting Input for Left Channel.
D2	INL–	Inverting Input for Left Channel.
D3	INR–	Inverting Input for Right Channel.
D4	INR+	Noninverting Input for Right Channel.

TYPICAL PERFORMANCE CHARACTERISTICS

EDGE pin = GND, unless otherwise noted.

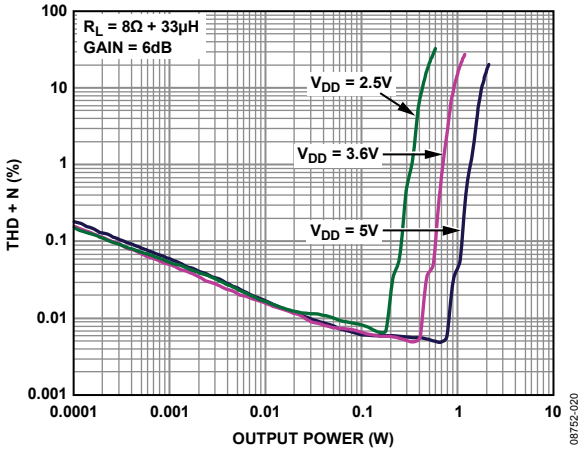

Figure 4. THD + N vs. Output Power into 8 Ω, Gain = 6 dB

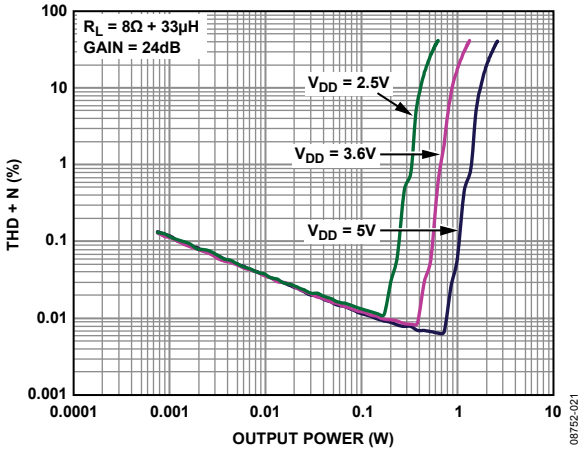

Figure 7. THD + N vs. Output Power into 8 Ω, Gain = 24 dB

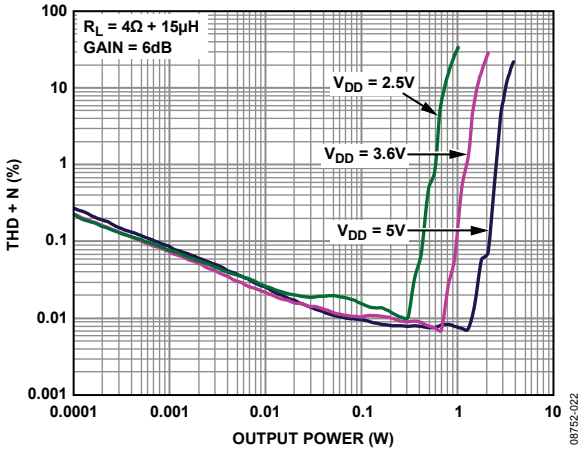

Figure 5. THD + N vs. Output Power into 4 Ω, Gain = 6 dB

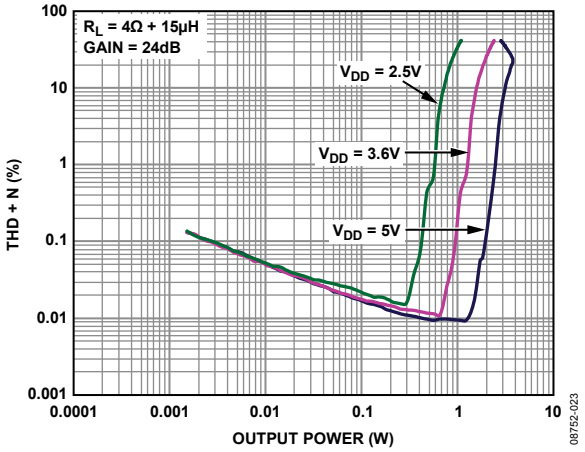

Figure 8. THD + N vs. Output Power into 4 Ω, Gain = 24 dB

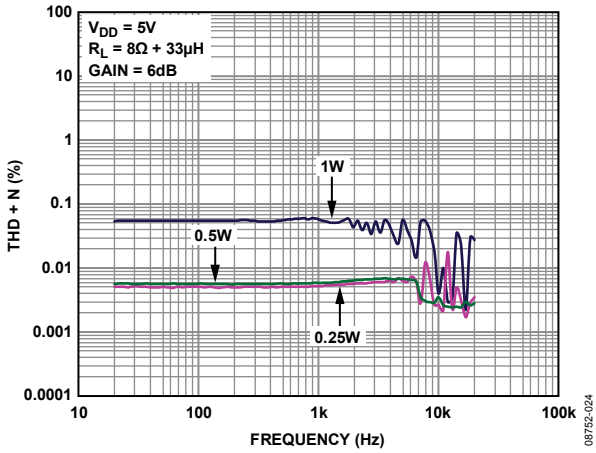

Figure 6. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, Gain = 6 dB

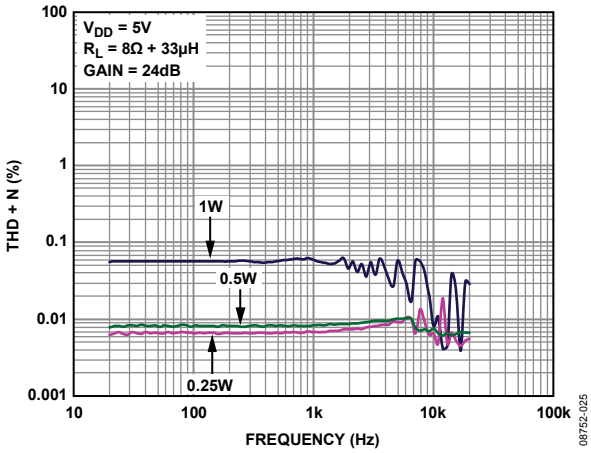

Figure 9. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, Gain = 24 dB

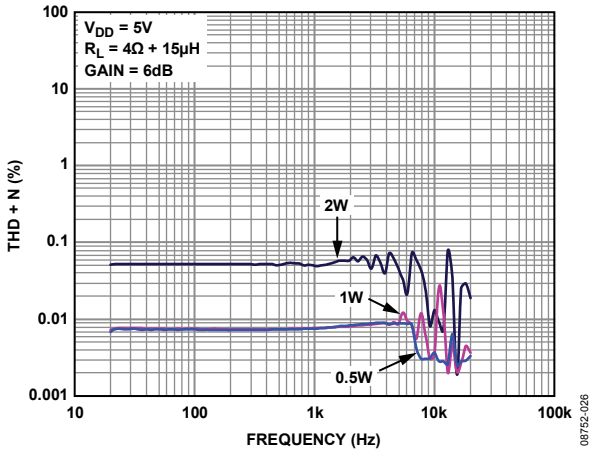

Figure 10. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, Gain = 6 dB

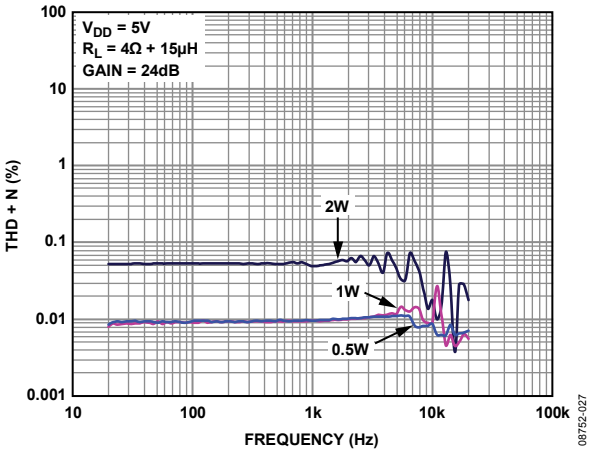

Figure 13. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, Gain = 24 dB

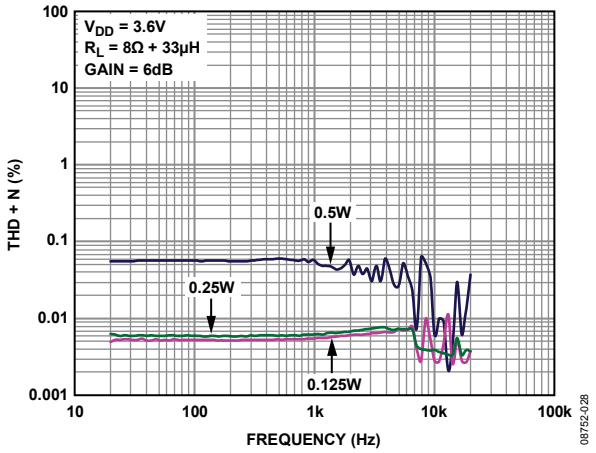

Figure 11. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, Gain = 6 dB

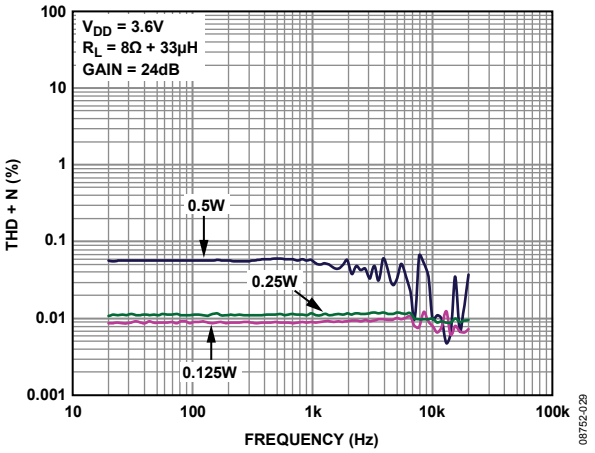

Figure 14. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, Gain = 24 dB

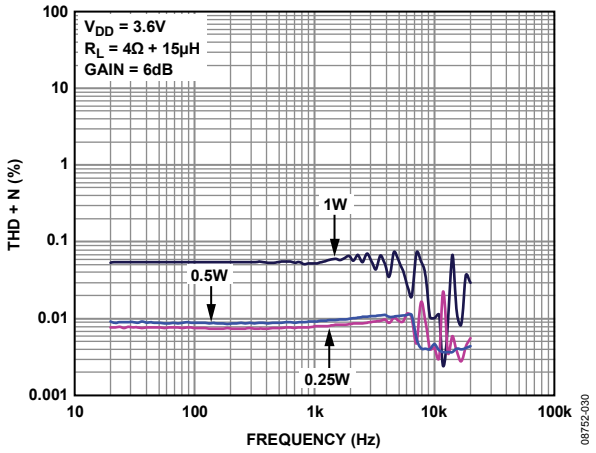

Figure 12. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, Gain = 6 dB

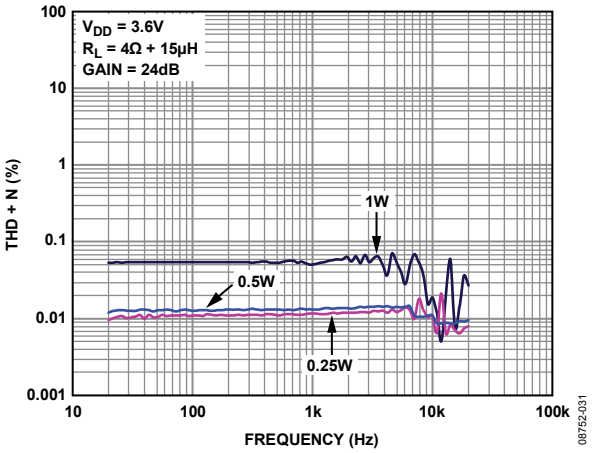

Figure 15. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, Gain = 24 dB

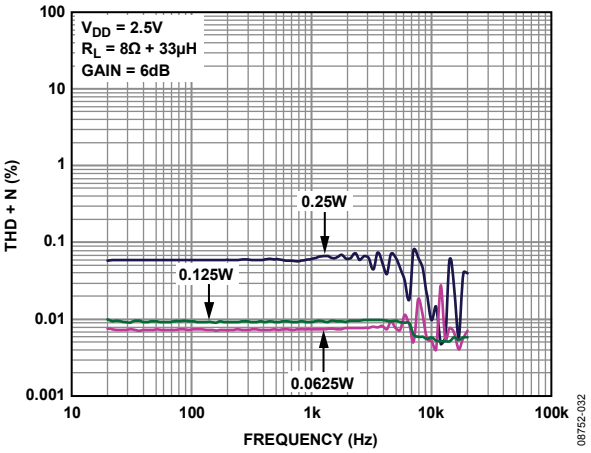

Figure 16. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, Gain = 6 dB

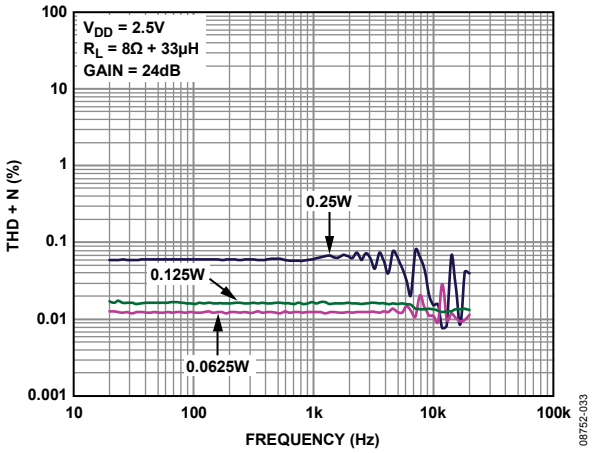

Figure 19. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, Gain = 24 dB

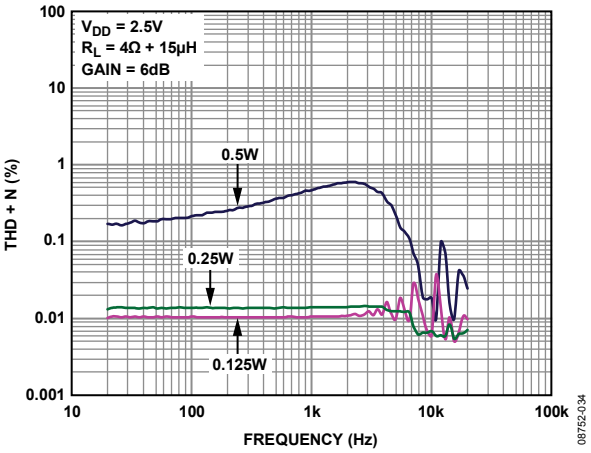

Figure 17. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, Gain = 6 dB

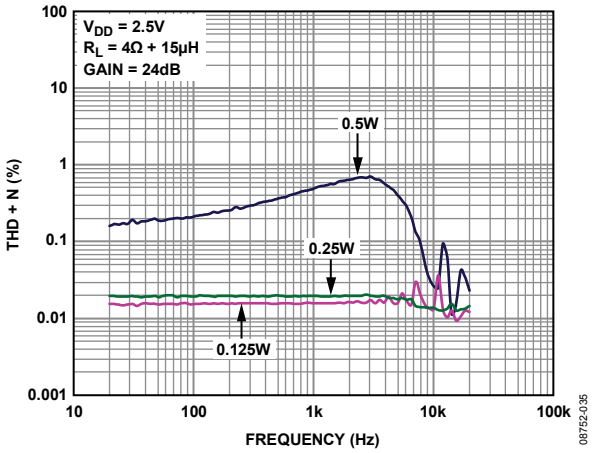

Figure 20. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, Gain = 24 dB

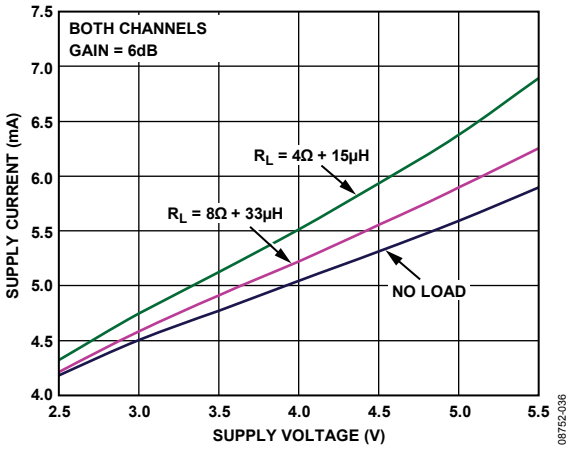

Figure 18. Supply Current vs. Supply Voltage, Gain = 6 dB

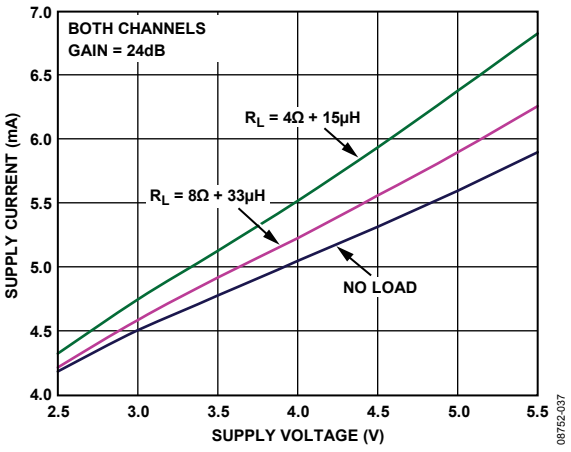

Figure 21. Supply Current vs. Supply Voltage, Gain = 24 dB

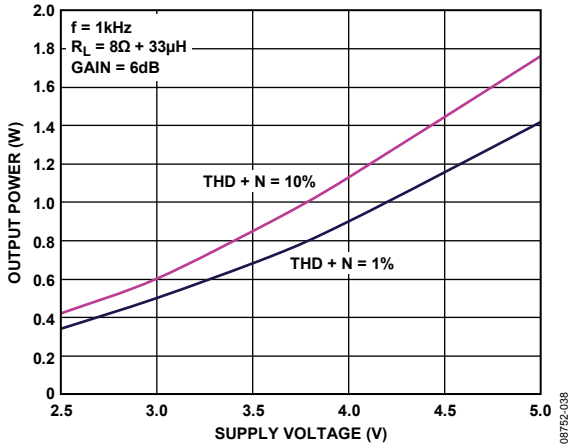

Figure 22. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, Gain = 6 dB

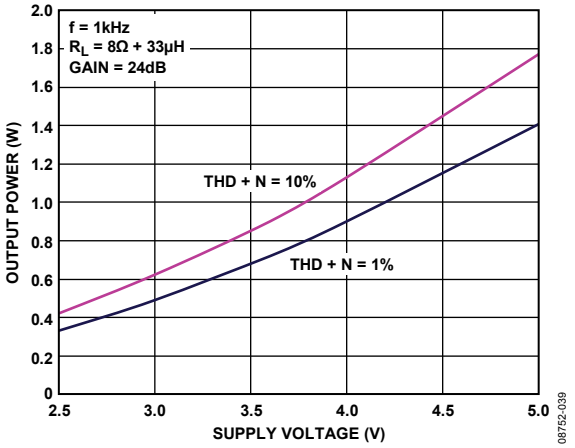

Figure 25. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, Gain = 24 dB

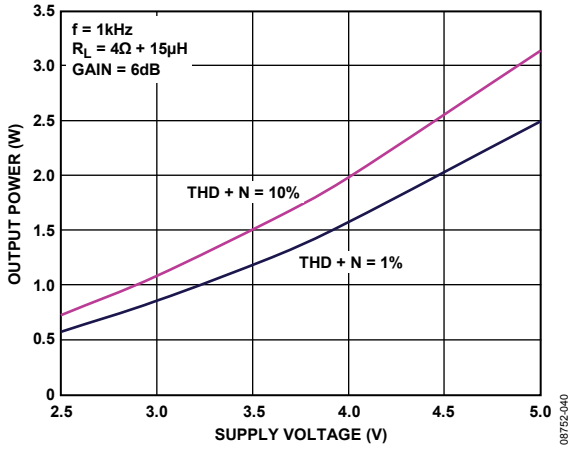

Figure 23. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, Gain = 6 dB

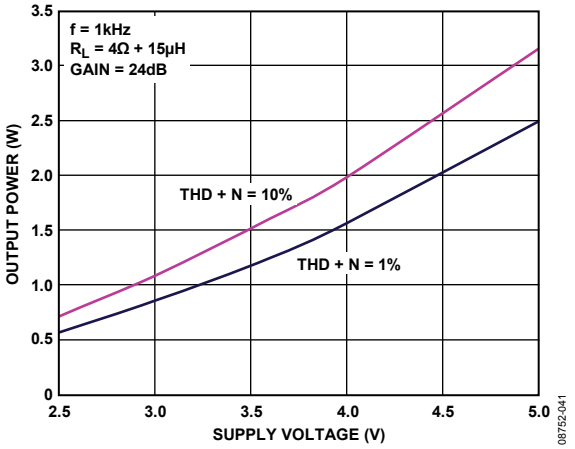

Figure 26. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, Gain = 24 dB

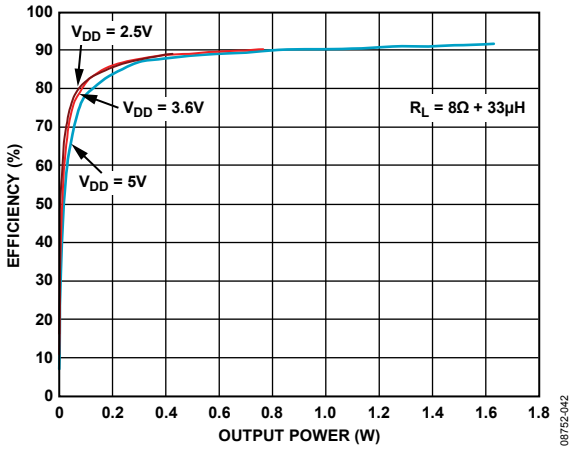

Figure 24. Efficiency vs. Output Power into 8 Ω

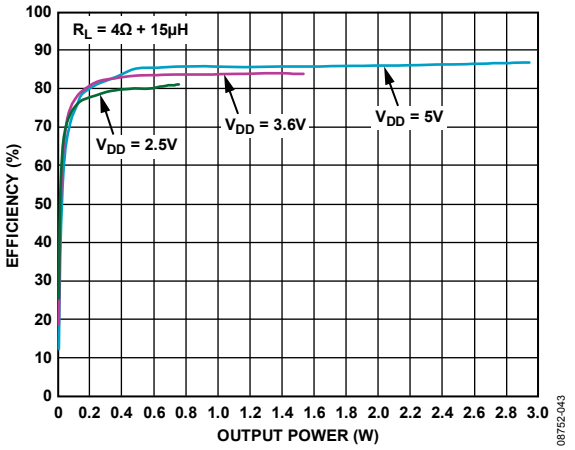

Figure 27. Efficiency vs. Output Power into 4 Ω

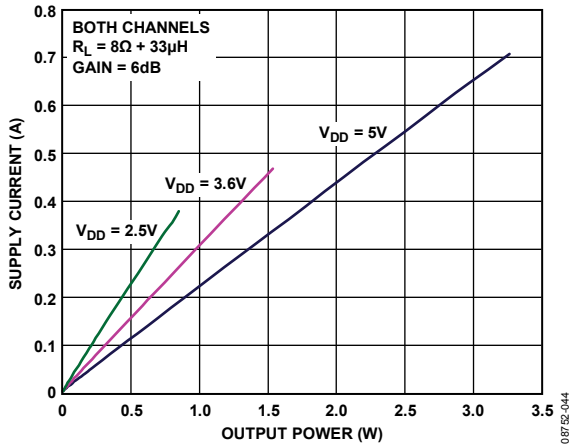

Figure 28. Supply Current vs. Output Power into 8 Ω

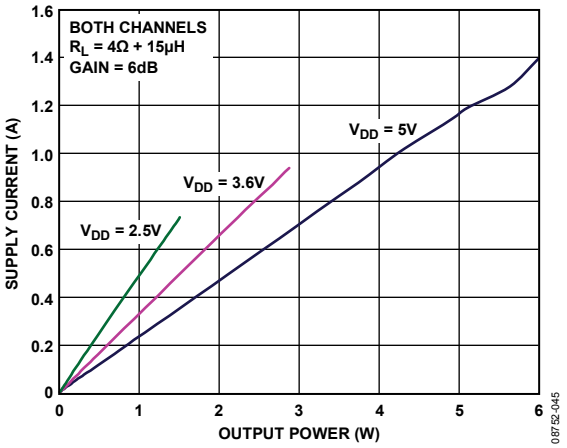

Figure 31. Supply Current vs. Output Power into 4 Ω

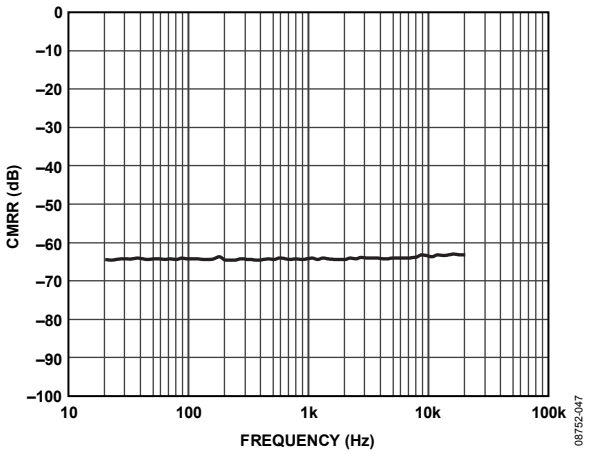

Figure 29. Common-Mode Rejection Ratio (CMRR) vs. Frequency

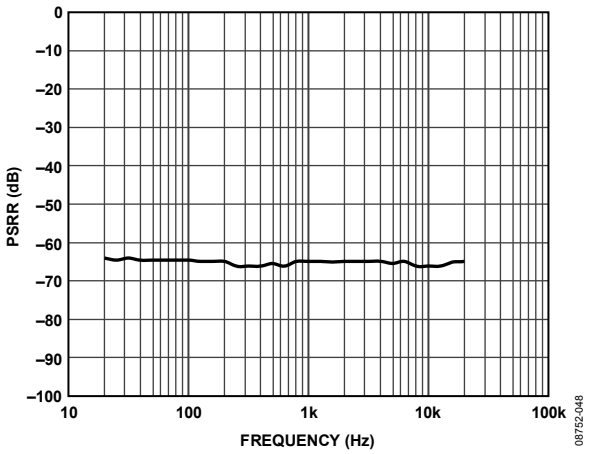

Figure 32. Power Supply Rejection Ratio (PSRR) vs. Frequency

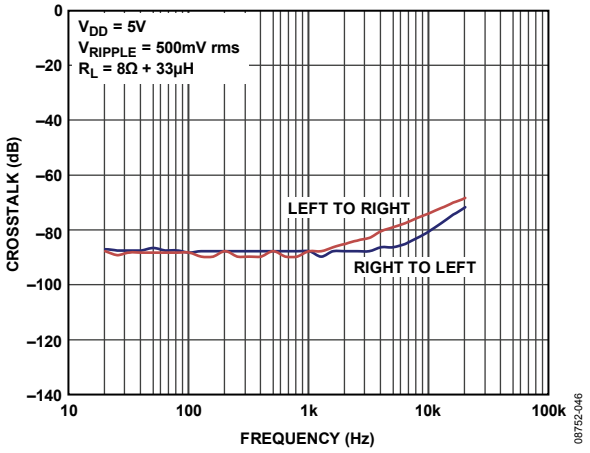

Figure 30. Crosstalk vs. Frequency

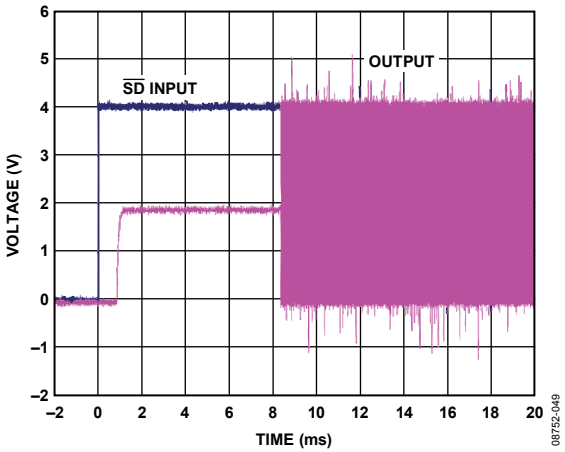

Figure 33. Turn-On Response

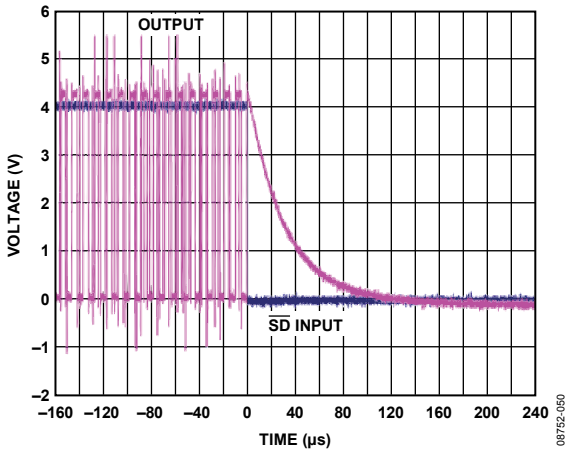

Figure 34. Turn-Off Response

THEORY OF OPERATION

OVERVIEW

The SSM2380 stereo, Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing system cost. The SSM2380 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2380 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits.

- Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do.
- Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emissions that might otherwise be radiated by speakers and long cable traces.
- The SSM2380 does not require external EMI filtering for twisted speaker cable lengths shorter than 10 cm. If longer speaker cables are used, the SSM2380 has an emission suppression mode that allows significantly longer speaker cable.
- Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for modulator synchronization is eliminated for designs that incorporate multiple SSM2380 amplifiers.

Using the I²C control interface, the gain of the SSM2380 can be selected from 1 dB to 24 dB (plus mute) in 47 steps with no external components and fixed input impedance. Other features accessed from the I²C interface include the following:

- Independent left/right channel shutdown
- Variable ultralow EMI emission control mode
- Automatic level control (ALC) for high quality speaker protection
- Stereo-to-mono mixing operation

The SSM2380 also offers protection circuits for overcurrent and overtemperature protection.

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients may be generated when the amplifier system changes its operating mode. For example, the following may be sources of audible transients: system power-up and power-down, mute and unmute, input source change, and sample rate change.

The SSM2380 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM2380 uses three-level, Σ-Δ output modulation. Each output can swing from GND to V_{DD} and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to the constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUTx+ and OUTx−) is generated to follow the input voltage. The differential pulse density (V_{OUT}) is increased by raising the input signal level. Figure 35 depicts three-level, Σ-Δ output modulation with and without input stimulus.

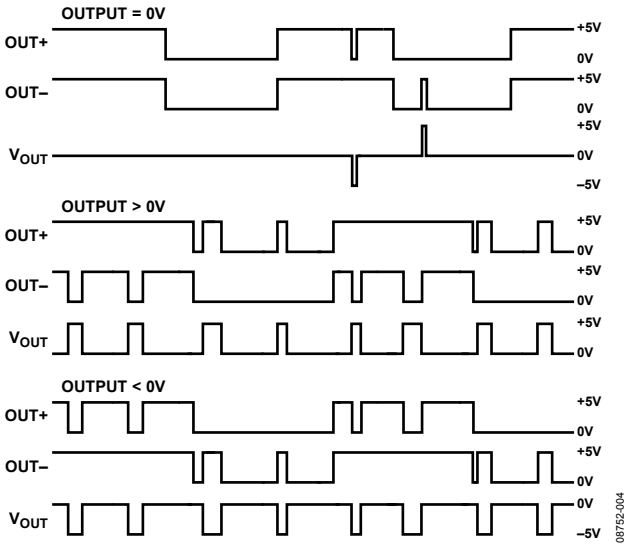

Figure 35. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

OPERATING MODES

The SSM2380 has three unique operating modes, controlled by the MODE pin. When MODE (Ball C2) is connected to GND, the SSM2380 operates in I²C control mode; Ball C3 and Ball C4 function as SCK and SDA for the I²C input. In I²C control mode, the user has full control of all internal registers of the SSM2380 (see Table 11).

When MODE (Ball C2) is connected to VDD, the SSM2380 operates in gain select mode; Ball C3 and Ball C4 function as the gain select pins, GAIN0 and GAIN1. All ALC and emission control features are disabled in gain select mode, and the user can set the gain to 6 dB, 12 dB, 18 dB, or 24 dB only.

When MODE (Ball C2) is not connected (floating), the SSM2380 operates in ALC mode; Ball C3 and Ball C4 function as EDGE and ALCTH. In ALC mode, the default gain is 18 dB. The user can enable or disable the emission control (EMI) feature by connecting EDGE (Ball C3) to VDD or GND. In addition to emission control, the ALC is activated. The user must connect a resistor from ALCTH (Ball C4) to GND. This resistor allows the user to limit the output level to any setting from 45% to 90% of V_{DD}.

Table 6. MODE Pin Selection Guide

SSM2380 Ball			
Ball C2 (MODE)	**Ball C3**	**Ball C4**	**Operating Mode**
High (connected to VDD)	GAIN0	GAIN1	Gain select mode
Low (connected to GND)	SCK	SDA	I²C control mode
Open (floating)	EDGE	ALCTH	ALC mode

ALC MODE OPERATION

When MODE is not connected (floating), the SSM2380 is in ALC mode, disabling the I²C interface. In ALC mode, the user has control of only two functions: setting the ALC threshold voltage and activating or deactivating the emission limiting circuitry.

Setting the ALC Threshold Voltage

To set the ALC threshold voltage, connect ALCTH (Ball C4) to GND with a series resistor. Figure 36 shows the relationship between the R_{TH} resistor setting and the output voltage limit as a percentage of the supply rail.

To calculate the resistor value, use the following equations:

$$Limit\ (\%) = 100 \times (R_{EXT} + 53)/(2.2 \times R_{EXT} + 58)\ k\Omega$$

$$R_{EXT} = (53 - 58 \times Limit/100)/(2.2 \times (Limit/100 - 1))\%$$

For example, to set an 80% limit,

$$R_{EXT} = (53 - 58 \times 80/100)/(2.2 \times (80/100 - 1)\ k\Omega$$

Therefore, 8.7 kΩ is required.

Maximum output power is derived from V_{TH} using the following equation:

$$P_{OUT} = \frac{\left(\frac{(Limit \times V_{DD})/100}{\sqrt{2}}\right)^2}{R_{SP}}$$

where R_{SP} is the speaker impedance.

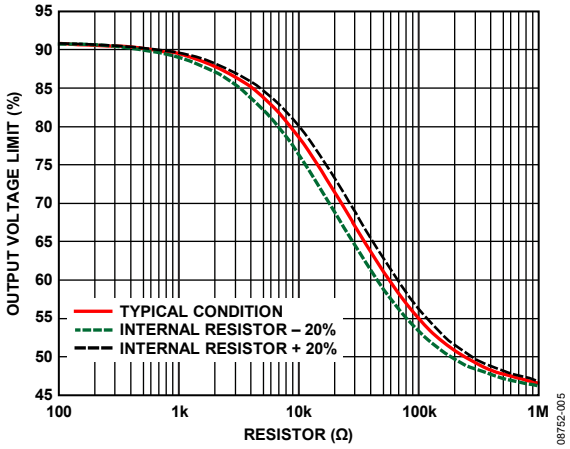

Figure 36. Output Voltage Limit (V_{TH}) vs. R_{TH}

In ALC mode, the attack, hold, and release times associated with ALC operation are at fixed levels, as indicated in Table 7.

Table 7. Attack, Hold, and Release Times for ALC Mode

Time	Duration
Attack Time	256 µs (per 0.5 dB step)
Hold Time	90 ms to 120 ms (nonadjustable)
Release Time	128 ms (per 0.5 dB step)

Activating or Deactivating the Emission Limiting Circuitry

To activate or deactivate the emission limiting circuitry, connect EDGE (Ball C3) to GND or to VDD. When EDGE is connected to GND, the SSM2380 is in normal operating mode, deactivating the emission limiting function. The device operates with maximum efficiency and noise level performance in this setting. The user can also pass FCC Class B emission testing with 10 cm twisted pair speaker wire for loudspeaker connection.

If longer speaker wire is desired, connect the EDGE pin to VDD to activate the emission limiting circuitry. The trade-off is slightly lower efficiency and noise performance. The penalty for using the emission control circuitry is far less than the decreased performance observed when using a ferrite bead based EMI filter for emission limiting purposes.

GAIN SELECT MODE OPERATION

When MODE is connected to VDD, the SSM2380 is in gain select mode, disabling the I²C interface. The ALC and emission limiting functions are also disabled. Ball C3 and Ball C4 function as the gain select pins, GAIN0 and GAIN1. Table 8 shows the user-selectable gain settings for the SSM2380.

Table 8. Gain Settings in Gain Select Mode

GAIN0 (Ball C3)	GAIN1 (Ball C4)	Gain Setting (dB)
GND	GND	6
VDD	GND	12
GND	VDD	18
VDD	VDD	24

I²C CONTROL MODE OPERATION

When MODE is connected to GND, the SSM2380 operates in I²C control mode, enabling Ball C3 and Ball C4 to act as SCK and SDA for the I²C input. In I²C control mode, the user has full control of all features of the SSM2380 (see Table 11).

- Gain control: 48-step, left/right independent control (ALC is off)
- ALC control (limiter/compressor): configurable attack and release times; configurable threshold voltage (16 level settings, 64% to 96% of V_{DD}); optional fixed-power mode (does not track rail)
- Output stage: active emissions edge rate control (four settings)
- Mixer: option to send left channel input to both left and right channel outputs or to send right channel input to both outputs

AUTOMATIC LEVEL CONTROL (ALC)

Automatic level control (ALC) is a function that automatically adjusts amplifier gain to generate the desired output amplitude with reference to a particular input stimulus. The primary use for the ALC is to protect an audio power amplifier or speaker load from the damaging effects of clipping or current overloading. This is accomplished by limiting the output amplitude of the amplifier upon reaching a preset threshold voltage. Another benefit of the ALC is that it makes sound sources with a wide dynamic range more intelligible by boosting low level signals, while in turn limiting very high level signals.

Before activating the ALC by setting the ALC_EN bit (Bit 7 in Register R4), the user has full control of the left and right channel PGA gain (programmable in Register R0 and Register R1). After the ALC is activated (ALC_EN = 1), the user has no control over the gain settings in Register R0 and Register R1; the left channel PGA gain is locked into the device and controls the gain for both the left and right channels. To change the gain, the user must reset the ALC_EN bit to 0 and then load the new gain settings.

Figure 37 shows the input vs. output and gain characteristics of the ALC that is implemented in the SSM2380.

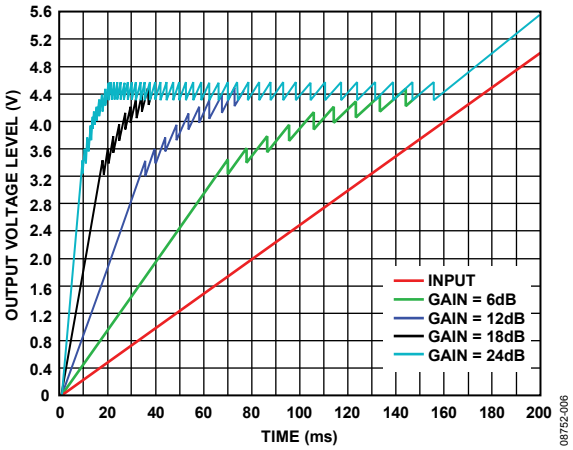

Figure 37. Input vs. Output and Gain Characteristics

When the input level is small and below the ALC threshold value, the gain of the amplifier stays at the preset gain setting. When the input exceeds the ALC threshold value, the ALC gradually reduces the gain from the preset gain setting down to 1 dB.

ALC Compression and Limiting Modes

The ALC implemented on the SSM2380 has two operation modes: compression and limiting. When the ALC is triggered for medium-level input signals, the ALC is in compression mode. In this mode, an increase of the output signal is one-third the increase of the input signal. For example, if the input signal increases by 3 dB, the ALC reduces the amplifier gain by 2 dB and thus the output signal increases by only 1 dB.

As the input signal becomes very large, the ALC transitions to limiting mode. In this mode, the output stays at a given threshold level, V_{TH}, even if the input signal grows larger. As an example of limiting mode operation, when a large input signal increases by 3 dB, the ALC reduces the amplifier gain by 3 dB and thus the output increases by 0 dB. When the amplifier gain is reduced to 1 dB, the ALC cannot reduce the gain further, and the output increases again. This is because the total range of the ALC operation has bottomed out due to extreme input voltage at high gain. To avoid potential speaker damage, the maximum input amplitude should not be large enough to exceed the maximum attenuation (to a level of 1 dB) of the limiting mode.

Attack Time, Hold Time, and Release Time

When the amplifier input signal exceeds a preset threshold, the ALC reduces amplifier gain rapidly until the output voltage settles to a target level. This target level is maintained for a certain period. If the input voltage does not exceed the threshold again, the ALC increases the gain gradually.

The attack time is the time taken to reduce the gain from maximum to minimum. The hold time is the time that the reduced gain is maintained. The release time is the time taken to increase the gain from minimum to maximum. These times are shown in Table 9.

Table 9. Attack, Hold, and Release Times for I²C Control Mode

Time[1]	Duration
Attack Time	32 µs to 4 ms (per 0.5 dB step)
Hold Time	90 ms to 120 ms
Release Time	4 ms to 512 ms (per 0.5 dB step)

[1] The attack time and release time can be adjusted using the I²C interface. The hold time cannot be adjusted.

Soft-Knee Compression

Often performed using sophisticated DSP algorithms, soft-knee compression provides maximum sound quality with effective speaker protection. Instead of using a fixed compression setting prior to limiting, the SSM2380 allows for a much more subtle transition into limiting mode, preserving the original sound quality of the source audio. Figure 38 to Figure 40 show the various soft-knee compression settings. If desired, compression can be disabled. When compression is disabled, the part operates in limiter-only mode.

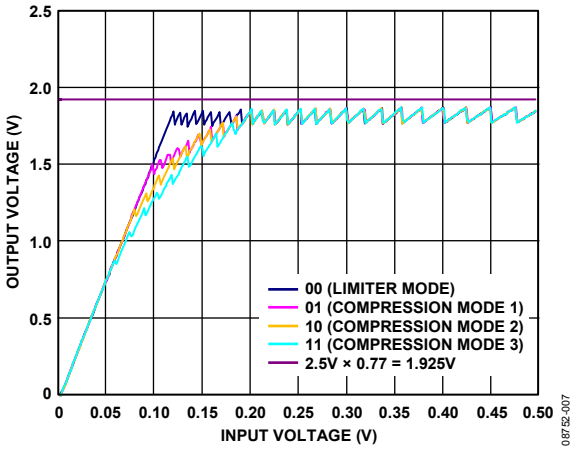

Figure 38. Adjustable Compression Settings, V_{DD} = 2.5 V, ALC Threshold Level = 77%

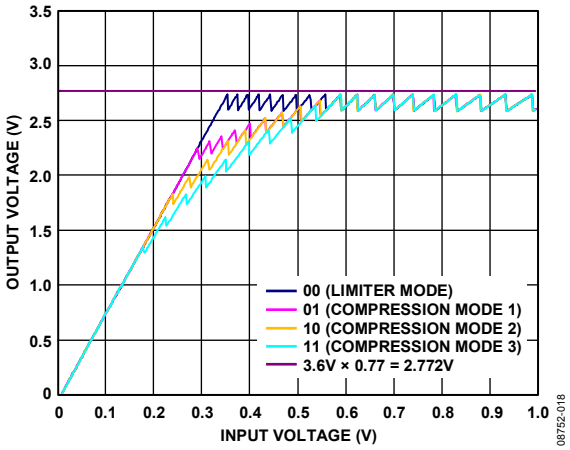

Figure 39. Adjustable Compression Settings, V_{DD} = 3.6 V, ALC Threshold Level = 77%

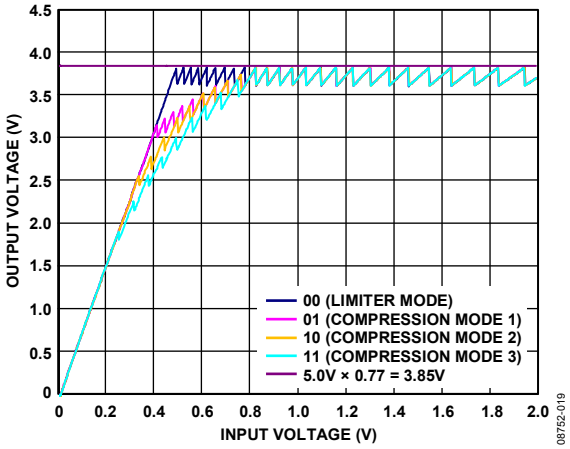

Figure 40. Adjustable Compression Setting, V_{DD} = 5.0 V, ALC Threshold Level = 77%

ALC Soft Transition

The ALC operation of the SSM2380 incorporates techniques to reduce the audible artifacts associated with gain change transitions. First, the gain is changed in small increments of 0.5 dB. In addition to this small step size, the rate of gain change is reduced, proportional to the attack time setting. This feature drastically reduces and virtually eliminates the presence of zipper noise and other artifacts associated with gain transitions during ALC operation. Figure 41 shows the soft transition operation.

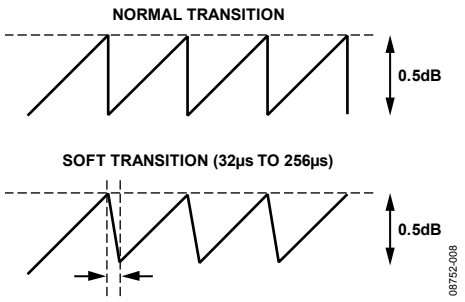

Figure 41. Soft Transition

MIXER MODE

When I²C control mode is activated, the user can send left channel input to both left and right channel outputs or send right channel input to both outputs. This is achieved by selecting Register R2, Bit 0 or Bit 1.

Using Mixer Mode with the ALC

If the ALC is enabled and the user also wishes to use the mixer operation, follow the guidelines in this section. Left channel gain controls the ALC; therefore, sending left channel input to the left and right channel outputs poses no problem for the ALC. However, to source the right channel input to the left and right channel outputs when using the ALC, the user must first load the left channel gain (Register R0, Bit 7).

With the ALC disabled, the user can also use the full mixer capability; that is, if the user wishes to mix the right and left inputs for both the right and left outputs, the ALC must be disabled. If the user needs both the mixing and ALC functions, the left or right channel must be muted to avoid problems.

When the ALC is active, the following options are acceptable:

- Left output = left input; right output = right input
- Left output = left input; right output = left input
- Left output = right input; right output = right input

To use the following options, the ALC must be disabled:

- Left output = left input + right input; right output = right input
- Left output = left input; right output = left input + right input
- Left output = left input + right input; right output = left input + right input

APPLICATIONS INFORMATION

LAYOUT

As output power increases, care must be taken to lay out printed circuit board (PCB) traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits. Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be directly beneath the analog power plane, and, similarly, the digital ground plane should be directly beneath the digital power plane. There should be no overlap between analog and digital ground planes or between analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2380 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the SSM2380 form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the dc PSRR performance.

In I²C control mode, the input impedance changes depending on the gain setting from Register R0 and Register R1 (LGAIN[5:0] and RGAIN[5:0] bits). Table 10 shows the R_{IN} value for each PGA gain setting.

Table 10. Input Impedance for I²C Control Mode

LGAIN[5:0], RGAIN[5:0]	Gain (dB)	R_{IN} (kΩ)
101110	24.0	7.3
101101	23.5	7.7
101100	23.0	8.1
101011	22.5	8.5
101010	22.0	9.0
101001	21.5	9.5
101000	21.0	10.0
100111	20.5	10.5
100110	20.0	11.1
100101	19.5	11.7
100100	19.0	12.3
100011	18.5	12.9
100010	18.0	13.6
100001	17.5	14.3
100000	17.0	15.0
011111	16.5	15.8
011110	16.0	16.6
011101	15.5	17.4
011100	15.0	18.3
011011	14.5	19.2
011010	14.0	20.1
011001	13.5	21.1
011000	13.0	22.1
010111	12.5	23.1
010110	12.0	24.2
010101	11.5	25.3
010100	11.0	26.4
010011	10.5	27.6
010010	10.0	28.8
010001	9.5	30.0
010000	9.0	31.3
001111	8.5	32.6
001110	8.0	34.0
001101	7.5	35.3
001100	7.0	36.7
001011	6.5	38.1
001010	6.0	39.6
001001	5.5	41.1
001000	5.0	42.6
000111	4.5	44.1
000110	4.0	45.6
000101	3.5	47.1
000100	3.0	48.7
000011	2.5	50.3
000010	2.0	51.8
000001	1.5	53.4
000000	1.0	55.0

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency is typically 325 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

The power supply inputs must be decoupled with a good quality, low ESL, low ESR capacitor, usually of approximately 4.7 µF. This capacitor bypasses low frequency noises to the ground plane.

For high frequency transient noises, use a 0.1 µF capacitor as close as possible to the VDD pins of the device. Placing the decoupling capacitors as close as possible to the SSM2380 helps to maintain efficient performance.

TYPICAL APPLICATION CIRCUITS

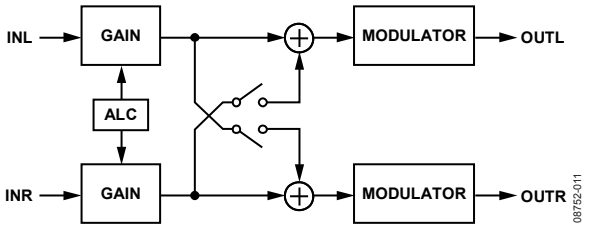

Figure 42. SSM2380 Mixer Operation Block Diagram

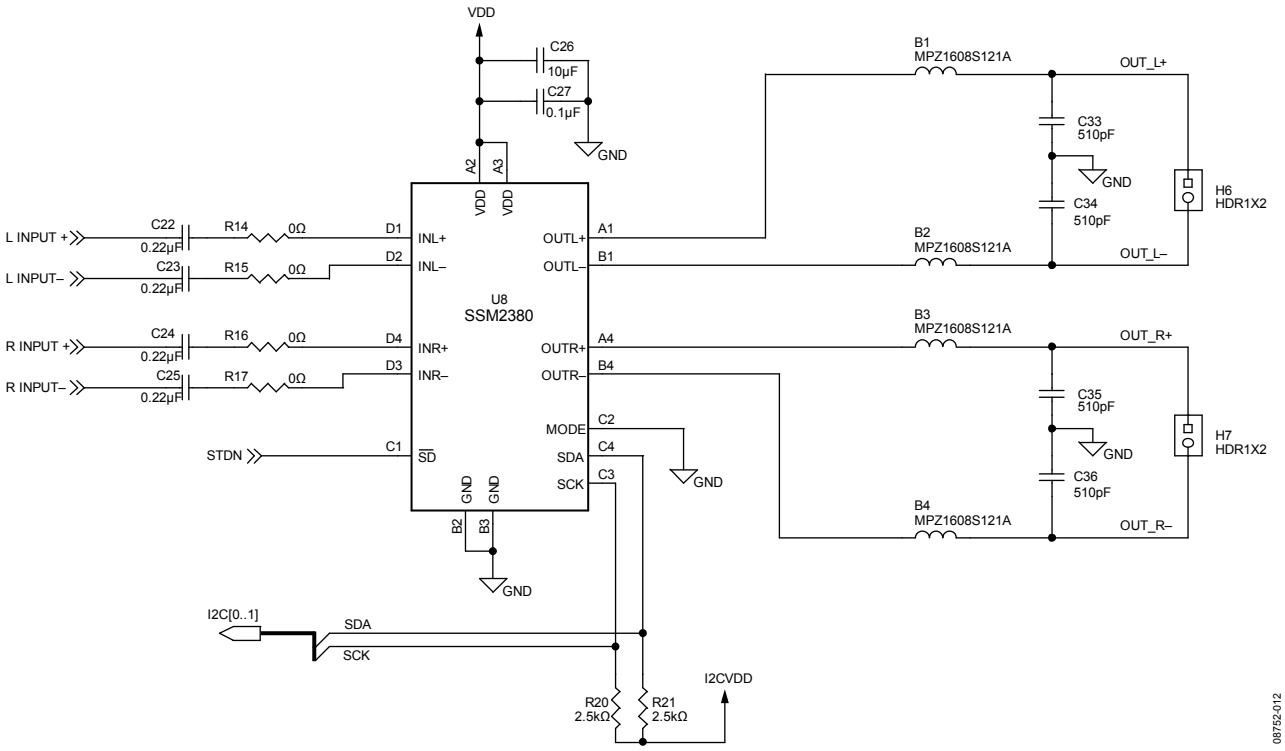

Figure 43. SSM2380 Typical Schematic, I²C Control Mode

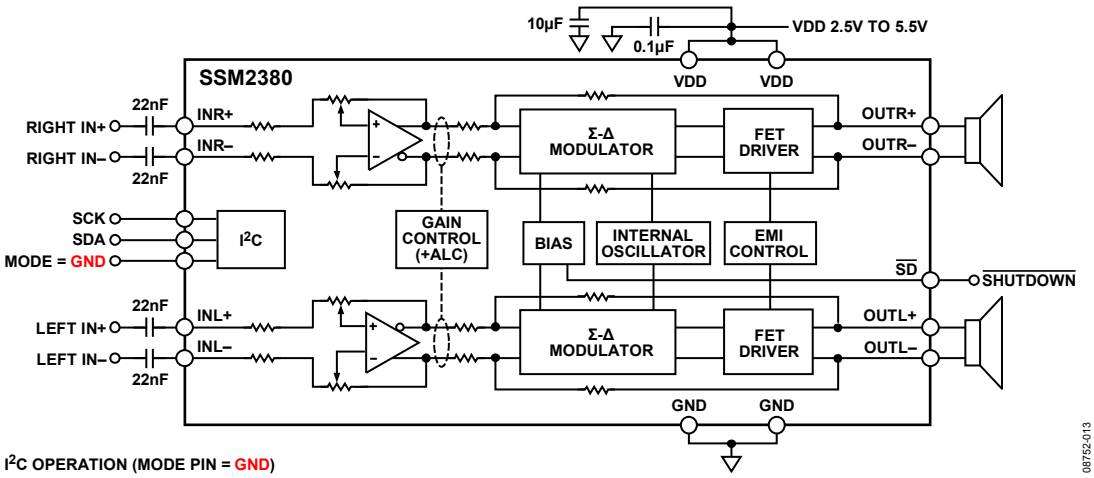

Figure 44. SSM2380 I²C Control Mode Configuration (MODE Pin = GND)

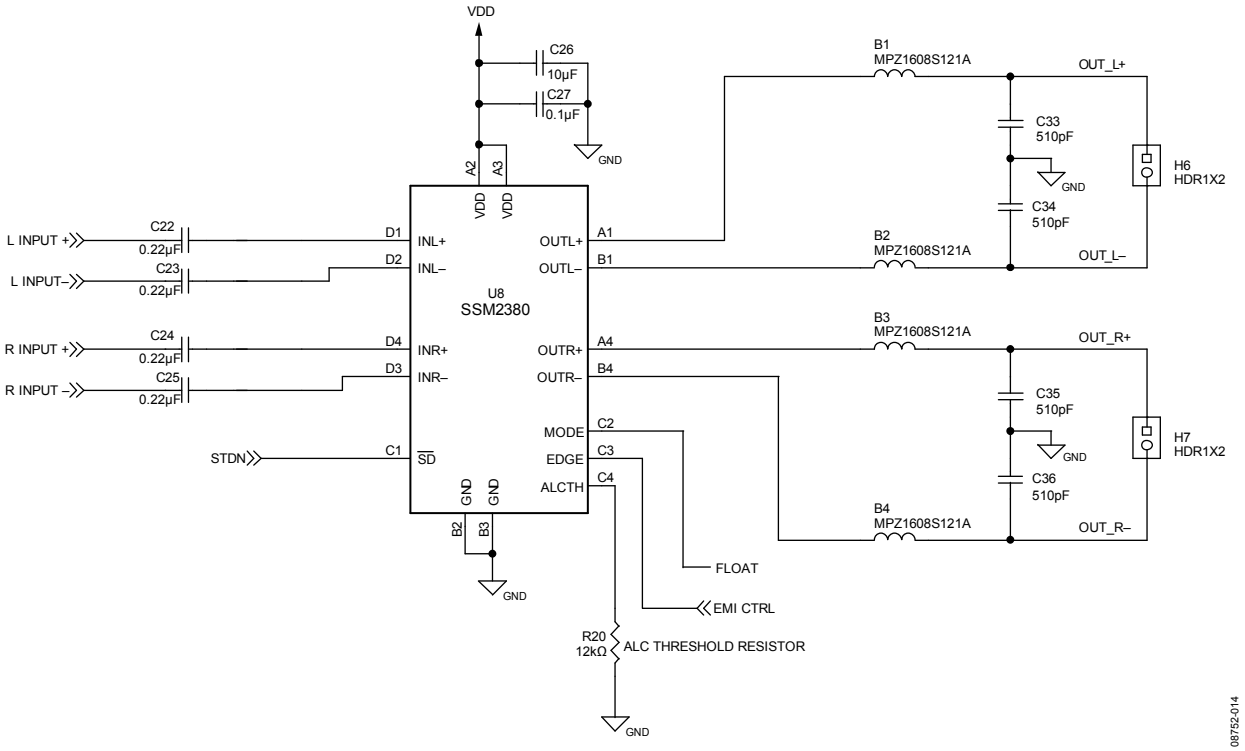

Figure 45. SSM2380 Typical Schematic, ALC Mode

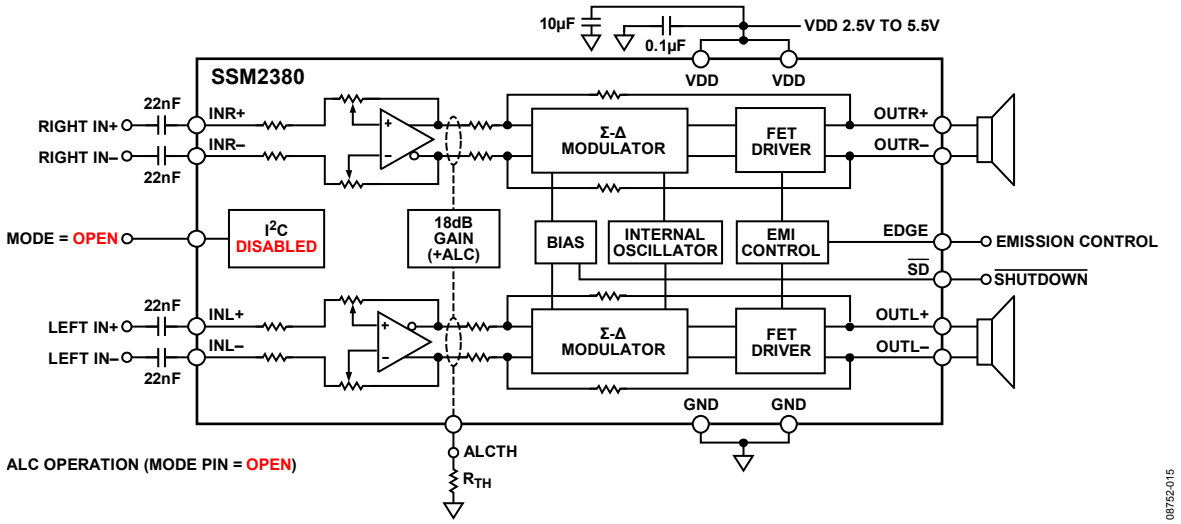

Figure 46. SSM2380 ALC Mode Configuration (MODE Pin = Open (Floating))

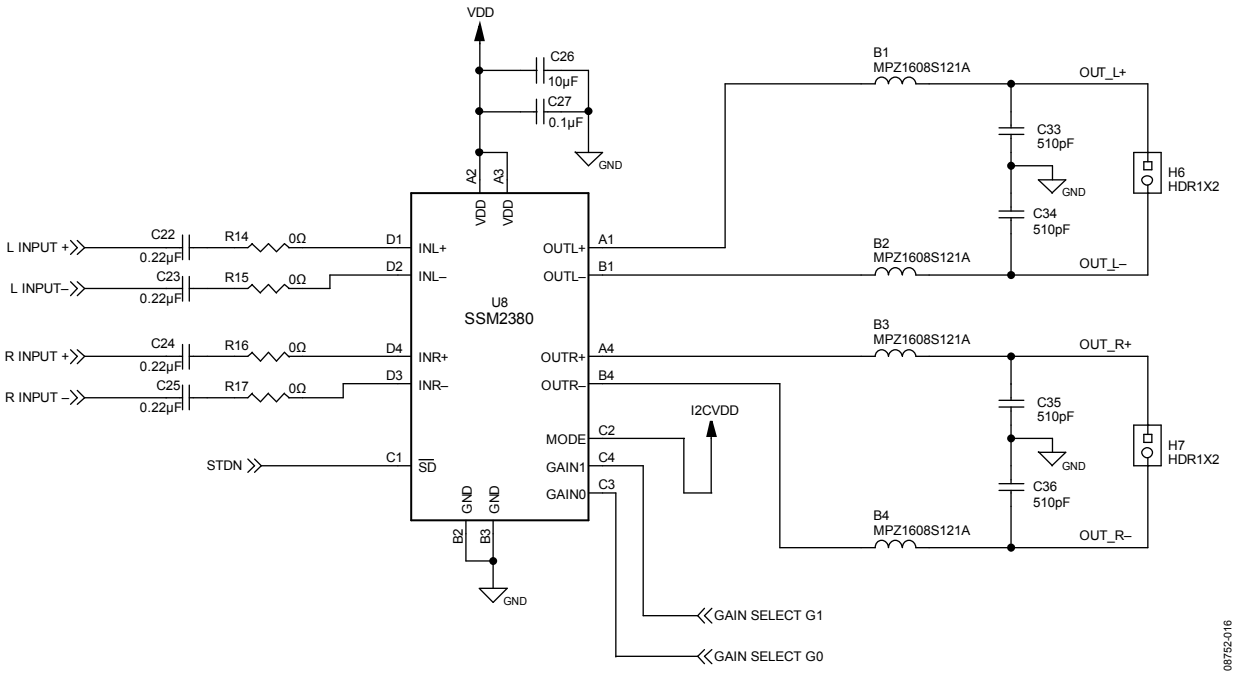

Figure 47. SSM2380 Typical Schematic, Gain Select Mode

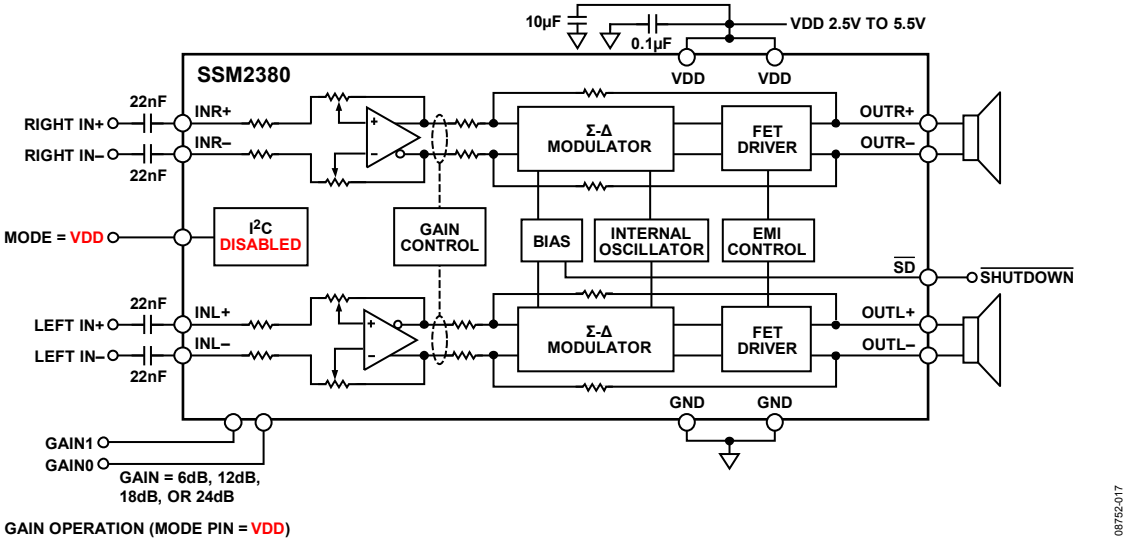

Figure 48. SSM2380 Gain Select Mode Configuration (MODE Pin = VDD)

I²C INTERFACE

The I²C interface provides access to the user-selectable control registers and operates with a 2-wire interface.

Each control register consists of 16 bits, MSB first. Bits[B15:B9] are the register map address, and Bits[B8:B0] are the register data for the associated register map.

SDA generates the serial control data-word, and SCK clocks the serial data. The I²C bus address (Bits[A7:A1]) is 0x31 (01100010 for write and 01100011 for read). Bit A0 is the designated read/write bit.

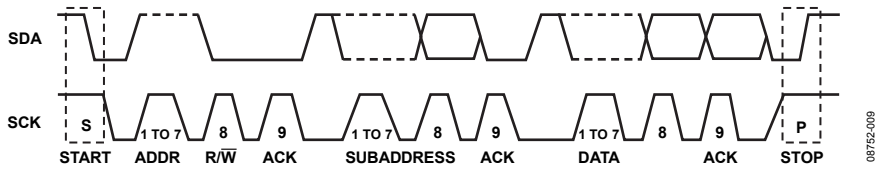

Figure 49. SSM2380 2-Wire I²C Generalized Clocking Diagram

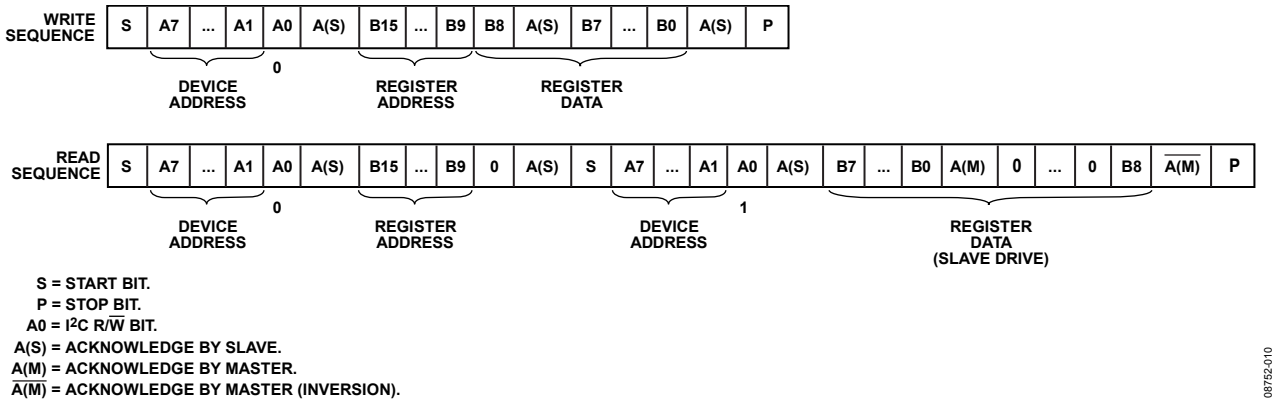

Figure 50. I²C Write and Read Sequences

REGISTER MAP

Table 11. Register Map

Reg	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
R0	0x00	Left channel gain control	LTOR	LMUTE	LGAIN[5:0]						00100010
R1	0x01	Right channel gain control	RTOL	RMUTE	RGAIN[5:0]						00100010
R2	0x02	Mode control	0	0	EDGE[1:0]		OCREC	OTREC	R2L	L2R	00001100
R3	0x03	ALC Control 1	0	0	RTIME[2:0]			LTIME[2:0]			00101011
R4	0x04	ALC Control 2	ALC_EN	COMP[1:0]		ALC_VFIX	ALCLV[3:0]				01001011
R5	0x05	Shutdown	0	0	0	0	0	0	STDNR	STDNL	00000011
R6	0x06	Error	0	0	0	0	OCR	OCL	OTW	OTP	00000000
R7	0x07	Error clear	0	0	0	0	0	0	0	0	00000000
R8	0x08	Reset	0	0	0	0	0	0	0	0	00000000

REGISTER MAP DETAILS

REGISTER R0: LEFT CHANNEL GAIN CONTROL, ADDRESS 0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LTOR	LMUTE	LGAIN[5:0]					

Table 12. Left Channel Gain Control Register Bit Descriptions

Bits	Bit Name	Description	
7	LTOR	Left-to-right channel gain data load control. 0 = disable simultaneous loading of left channel gain data to left and right channel registers (default). 1 = enable simultaneous loading of left channel gain data to left and right channel registers.	
6	LMUTE	Left channel input mute. 0 = disable mute (default). 1 = enable mute on left channel amplifier.	
[5:0]	LGAIN[5:0]	Left channel gain control. Each step represents a 0.5 dB increase in gain. For ALC operation, these bits control the gain setting for both the left and right channels. If the ALC_EN bit in Register R4 is set to 1, these bits cannot be changed.	
		Setting	**Gain**
		000000	1 dB
		…	…
		100010	18 dB (default)
		…	…
		101101	23.5 dB
		101110 to 111111	24 dB

REGISTER R1: RIGHT CHANNEL GAIN CONTROL, ADDRESS 0x01

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTOL	RMUTE	RGAIN[5:0]					

Table 13. Right Channel Gain Control Register Bit Descriptions

Bits	Bit Name	Description	
7	RTOL	Right-to-left channel gain data load control. 0 = disable simultaneous loading of right channel gain data to left and right channel registers (default). 1 = enable simultaneous loading of right channel gain data to left and right channel registers.	
6	RMUTE	Right channel input mute. 0 = disable mute (default). 1 = enable mute on right channel amplifier.	
[5:0]	RGAIN[5:0]	Right channel gain control. Each step represents a 0.5 dB increase in gain. If the ALC_EN bit in Register R4 is set to 1, these bits cannot be changed.	
		Setting	**Gain**
		000000	1 dB
		…	…
		100010	18 dB (default)
		…	…
		101101	23.5 dB
		101110 to 111111	24 dB

REGISTER R2: MODE CONTROL, ADDRESS 0x02

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	EDGE[1:0]		OCREC	OTREC	R2L	L2R

Table 14. Mode Control Register Bit Descriptions

Bits	Bit Name	Description	
[5:4]	EDGE[1:0]	Edge rate control.	
		Setting	**Rate Control**
		00	Normal mode (default)
		01	Slow edge
		10	Slow edge (V_{DD} > 3.0 V recommended)
		11	Slow edge (V_{DD} > 4.0 V recommended)
3	OCREC	Overcurrent autorecovery enable. 0 = disabled. 1 = enabled (default).	
2	OTREC	Overtemperature autorecovery enable. 0 = disabled. 1 = enabled (default).	
1	R2L	Right channel signal mix enable (send right channel input to left and right channel outputs). 0 = mix disabled (default). 1 = mix enabled.	
0	L2R	Left channel signal mix enable (send left channel input to left and right channel outputs). 0 = mix disabled (default). 1 = mix enabled.	

REGISTER R3: ALC CONTROL 1, ADDRESS 0x03

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RTIME[2:0]			LTIME[2:0]		

Table 15. ALC Control 1 Register Bit Descriptions

Bits	Bit Name	Description	
[5:3]	RTIME[2:0]	Release time setting (0.5 dB step).	
		Setting	**Release Time**
		000	4 ms/step (6 dB/48 ms)
		001	8 ms/step
		010	16 ms/step
		011	32 ms/step
		100	64 ms/step
		101	128 ms/step (default)
		110	256 ms/step
		111	512 ms/step
[2:0]	LTIME[2:0]	Attack time setting (0.5 dB step).	
		Setting	**Attack Time**
		000	32 µs/step (6 dB/384 µs)
		001	64 µs/step
		010	128 µs/step
		011	256 µs/step (default)
		100	512 µs/step
		101	1 ms/step
		110	2 ms/step
		111	4 ms/step

REGISTER R4: ALC CONTROL 2, ADDRESS 0x04

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ALC_EN	COMP[1:0]		ALC_VFIX	ALCLV[3:0]			

Table 16. ALC Control 2 Register Bit Descriptions

Bits	Bit Name	Description	
7	ALC_EN	ALC enable (gain setting loaded to ALC control). 0 = disabled (default). 1 = enabled.	
[6:5]	COMP[1:0]	Compressor setting.	
		Setting	**Compression**
		00	Limiter mode (1:∞)
		01	Compression Mode 1 (1:4 to 1:∞)
		10	Compression Mode 2 (1:1.7 to 1:4 to 1:∞) (default)
		11	Compression Mode 3 (1:2 to 1:2.5 to 1:∞)
4	ALC_VFIX	ALC threshold mode setting. 0 = supply tracking (default). 1 = fixed power.	
[3:0]	ALCLV[3:0]	ALC threshold level setting. See Table 17 for a complete list of the settings (default value is 1011).	

Table 17. ALC Threshold Level Settings

ALCLV[3:0]	Supply Tracking Mode (ALC_VFIX = 0)	Fixed Power Mode (ALC_VFIX = 1)		
Value	**% of V_{DD}**	**Voltage Limit (V)**	**Power, 8 Ω Load (W)**	**Power, 4 Ω Load (W)**
1111	96	4.36	1.19	2.38
1110	93	4.25	1.13	2.25
1101	90	4.13	1.06	2.13
1100	88	4.01	1.0	2.01
1011	85	3.89	0.95	1.89
1010	83	3.77	0.89	1.78
1001	80	3.65	0.83	1.67
1000	78	3.54	0.78	1.56
0111	76	3.42	0.73	1.46
0110	74	3.30	0.68	1.36
0101	72	3.18	0.63	1.27
0100	70	3.06	0.59	1.17
0011	69	2.95	0.54	1.09
0010	67	2.83	0.50	1.00
0001	66	2.71	0.46	0.92
0000	64	2.59	0.42	0.84

REGISTER R5: SHUTDOWN, ADDRESS 0x05

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	STDNR	STDNL

Table 18. Shutdown Register Bit Descriptions

Bits	Bit Name	Description
1	STDNR	Right channel shutdown control. 0 = power up right channel. 1 = power down right channel (default).
0	STDNL	Left channel shutdown control. 0 = power up left channel. 1 = power down left channel (default).

REGISTER R6: ERROR, ADDRESS 0x06

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	OCR	OCL	OTW	OTP

Table 19. Error Register Bit Descriptions (Read-Only Register)

Bits	Bit Name	Description
3	OCR	Overcurrent error bit, right channel. 0 = no error detected (default). 1 = error state flagged (if OCREC bit in the mode control register is set to 1).
2	OCL	Overcurrent error bit, left channel. 0 = no error detected (default). 1 = error state flagged (if OCREC bit in the mode control register is set to 1).
1	OTW	Overtemperature warning bit. 0 = no error detected (default). 1 = warning state flagged (if OTREC bit in the mode control register is set to 1).
0	OTP	Overtemperature error bit. 0 = no error detected (default). 1 = error state flagged (if OTREC bit in the mode control register is set to 1).

REGISTER R7: ERROR CLEAR, ADDRESS 0x07

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0

Table 20. Error Clear Register Bit Descriptions

Bits	Bit Name	Description
[7:0]	Error clear	Recovery from error condition. Used when autorecovery is disabled.

REGISTER R8: RESET, ADDRESS 0x08

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0

Table 21. Reset Register Bit Descriptions

Bits	Bit Name	Description
[7:0]	Reset	Clear all registers to their default values. Used when autorecovery is disabled.

OUTLINE DIMENSIONS

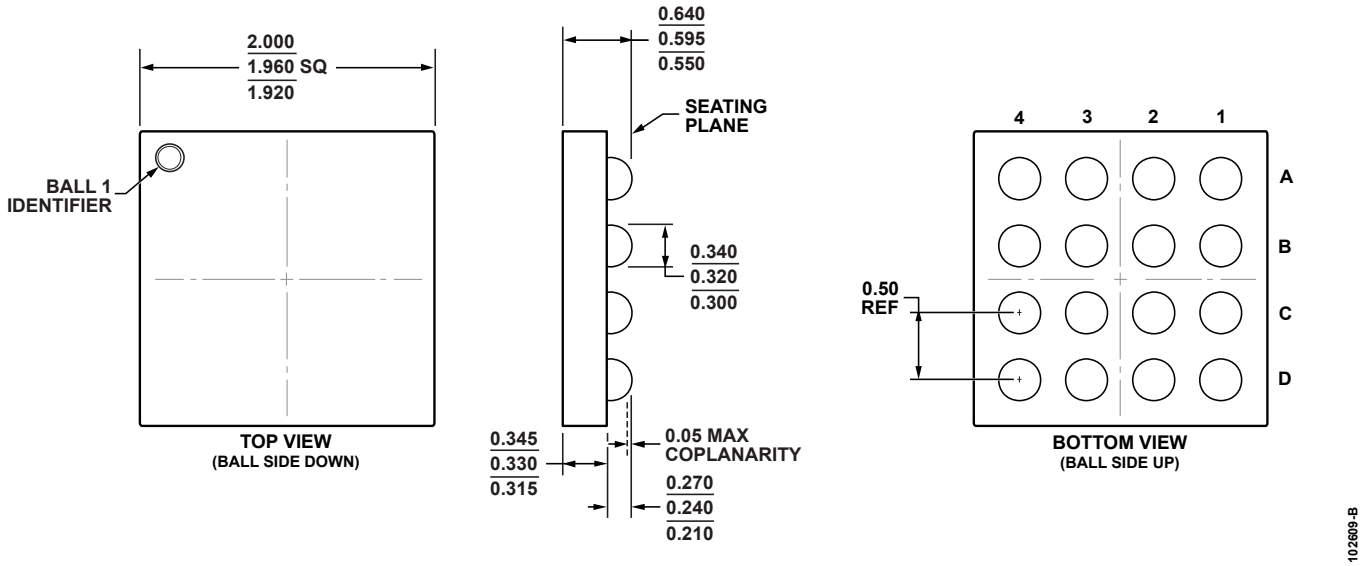

Figure 51. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2380CBZ-REEL	−40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-3
SSM2380CBZ-REEL7	−40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-3
EVAL-SSM2380Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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