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REVISION HISTORY

11/05—Rev. B to Rev. C

Updated Format	Universal
Changes to Table 4.....	6
Updated Outline Dimensions	17
Changes to Ordering Guide	17

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	B Version ¹			Unit	Test Conditions/Comments
	Min	Typ	Max		
STATIC PERFORMANCE ²					
Resolution	12			Bits	See Figure 5 Guaranteed monotonic by design (see Figure 6) All zeroes loaded to DAC register (see Figure 9) All ones loaded to DAC register (see Figure 9)
Relative Accuracy			±16	LSB	
Differential Nonlinearity			±1	LSB	
Zero-Code Error		5	40	mV	
Full-Scale Error		−0.15	−1.25	% of FSR	
Gain Error			±1.25	% of FSR	
Zero-Code Error Drift		−20		μV/°C	
Gain Temperature Coefficient		−5		ppm of FSR/°C	
OUTPUT CHARACTERISTICS ³					
Output Voltage Range	0		V _{DD}	V	1/4 scale to 3/4 scale change (400 hex to C00 hex) R _L = 2 kΩ, 0 pF < C _L < 200 pF (see Figure 19) R _L = 2 kΩ, C _L = 500 pF R _L = ∞ R _L = 2 kΩ 1 LSB change around major carry (see Figure 22) V _{DD} = 5 V V _{DD} = 3 V Coming out of power-down mode, V _{DD} = 5 V Coming out of power-down mode, V _{DD} = 3 V
Output Voltage Settling Time		8	10	μs	
		12		μs	
Slew Rate		1		V/μs	
Capacitive Load Stability		470		pF	
		1000		pF	
Digital-to-Analog Glitch Impulse		20		nV-s	
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1		Ω	
Short Circuit Current		50		mA	
		20		mA	
Power-Up Time		2.5		μs	
		5		μs	
LOGIC INPUTS ³					
Input Current			±1	μA	V _{DD} = 5 V V _{DD} = 3 V V _{DD} = 5 V V _{DD} = 3 V
V _{INL} , Input Low Voltage			0.8	V	
V _{INL} , Input Low Voltage			0.6	V	
V _{INH} , Input High Voltage	2.4			V	
V _{INH} , Input High Voltage	2.1			V	
Pin Capacitance			3	pF	
POWER REQUIREMENTS					
V _{DD}	2.7		5.5	V	DAC active and excluding load current V _{IH} = V _{DD} and V _{IL} = GND V _{IH} = V _{DD} and V _{IL} = GND V _{IH} = V _{DD} and V _{IL} = GND V _{IH} = V _{DD} and V _{IL} = GND
I _{DD} (Normal Mode)					
V _{DD} = 4.5 V to 5.5 V		140	250	μA	
V _{DD} = 2.7 V to 3.6 V		115	200	μA	
I _{DD} (All Power-Down Modes)					
V _{DD} = 4.5 V to 5.5 V		0.2	1	μA	
V _{DD} = 2.7 V to 3.6 V		0.05	1	μA	
POWER EFFICIENCY					
I _{OUT} /I _{DD}		93		%	I _{LOAD} = 2 mA, V _{DD} = 5 V

¹ Temperature range is as follows: B Version: -40°C to $+105^\circ\text{C}$.

² Linearity calculated using a reduced code range of 48 to 4047; output unloaded.

³ Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$, all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter ^{1, 2}	Limit at T_{MIN} , T_{MAX}		Unit	Description
	$V_{DD} = 2.7\text{ V to }3.6\text{ V}$	$V_{DD} = 3.6\text{ V to }5.5\text{ V}$		
t_1^3	50	33	ns min	SCLK cycle time
t_2	13	13	ns min	SCLK high time
t_3	22.5	13	ns min	SCLK low time
t_4	0	0	ns min	$\overline{\text{SYNC}}$ to SCLK rising edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	50	33	ns min	Minimum $\overline{\text{SYNC}}$ high time

¹ All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

² See Figure 2.

³ Maximum SCLK frequency is 30 MHz at $V_{DD} = 3.6\text{ V to }5.5\text{ V}$ and 20 MHz at $V_{DD} = 2.7\text{ V to }3.6\text{ V}$.

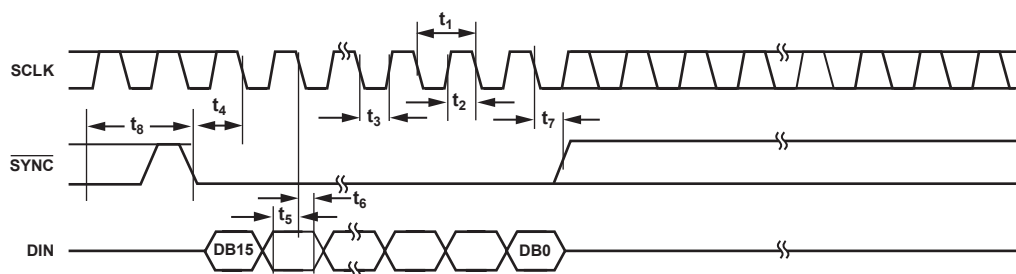


Figure 2. Serial Write Operation

00934-002

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Ratings
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to $V_{DD} + 0.3$ V
V_{OUT} to GND	−0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Industrial (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Max)	150°C
SOT-23 Package	
Power Dissipation	$(T_J \text{ Max} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
MSOP Package	450 mW
Power Dissipation	$(T_J \text{ Max} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD5320

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

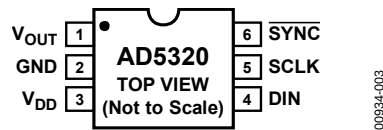
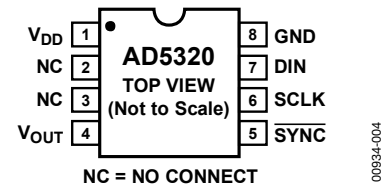


Figure 3. SOT-23 Pin Configuration



NC = NO CONNECT

Figure 4. MSOP Pin Configuration

Table 4. Pin Function Descriptions

SOT-23 Pin No.	MSOP Pin No.	Mnemonic	Description
1	4	V _{OUT}	Analog Output Voltage from DAC. The output amplifier has rail-to-rail operation.
2	8	GND	Ground Reference Point for All Circuitry on the Part.
3	1	V _{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V and V _{DD} should be decoupled to GND.
4	7	DIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
5	6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
6	5	SYNC	Level Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When SYNC goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless SYNC is taken high before this edge, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC.
	2, 3	NC	No Connect.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 5.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 6.

Zero-Code Error

Zero-code error is a measure of the output error when zero code (000 hex) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5320 because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 9.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFF Hex) is loaded to the DAC register. Ideally the output should be $V_{DD} - 1$ LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 9.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error

Total unadjusted error (TUE) is a measure of the output error considering all the various errors. A typical TUE vs. code plot can be seen in Figure 7.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/ $^\circ\text{C}$.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV seconds and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FF Hex to 800 Hex); see Figure 22.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV seconds and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

TYPICAL PERFORMANCE CHARACTERISTICS

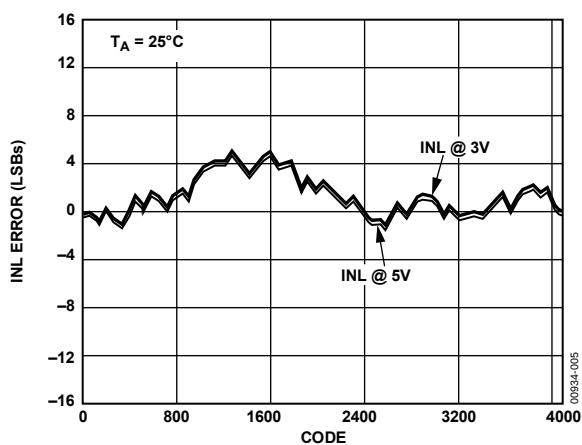


Figure 5. Typical INL Plot

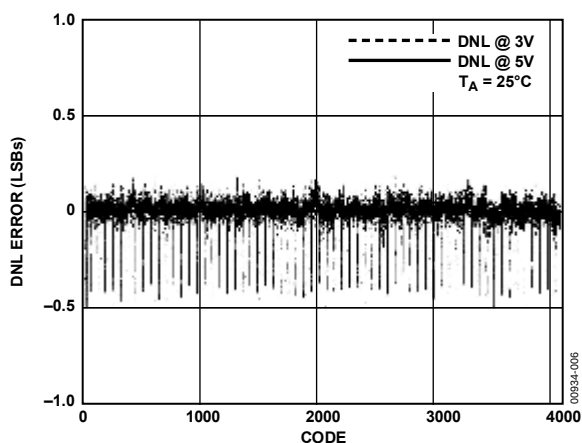


Figure 6. Typical DNL Plot

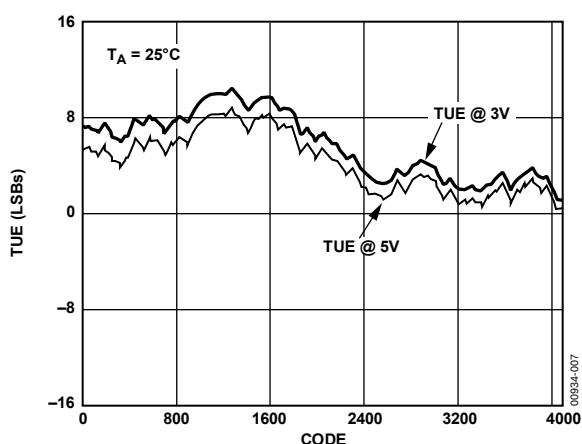


Figure 7. Typical Total Unadjusted Error Plot

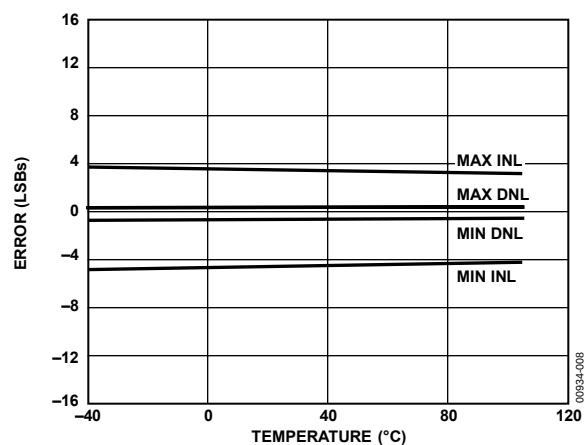


Figure 8. INL Error and DNL Error vs. Temperature

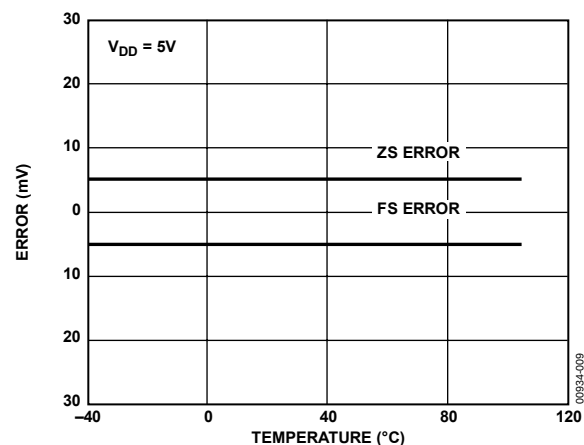
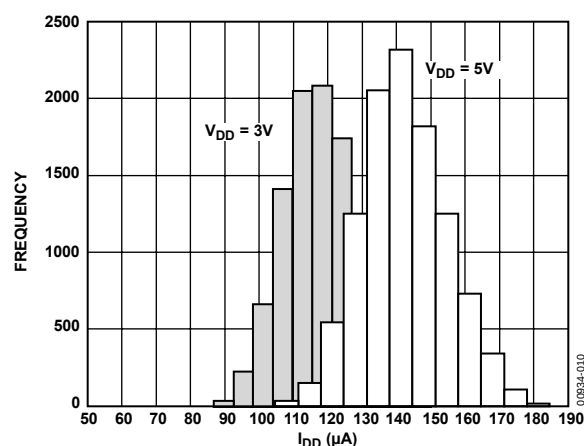


Figure 9. Zero-Scale Error and Full-Scale Error vs. Temperature

Figure 10. I_{DD} Histogram with $V_{DD} = 3\text{ V}$ and $V_{DD} = 5\text{ V}$

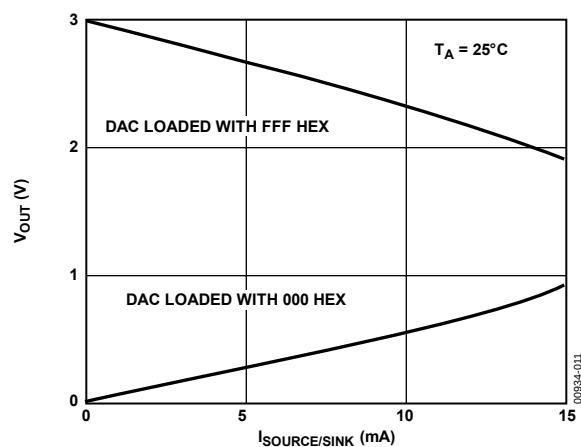
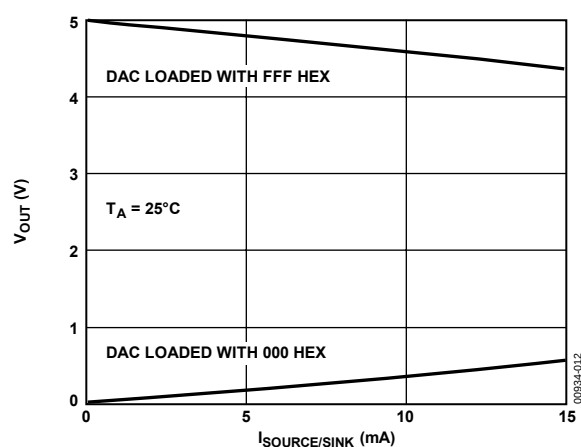
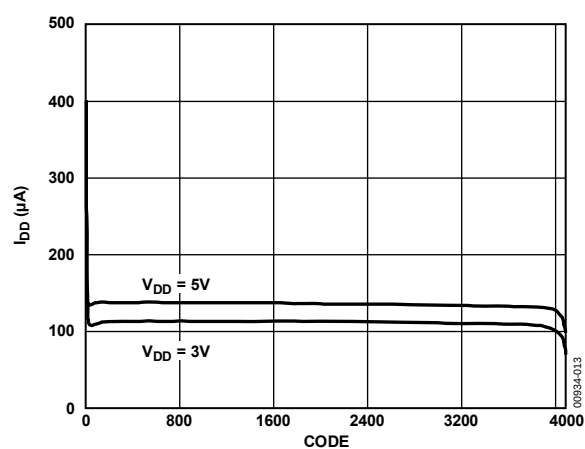
Figure 11. Source and Sink Current Capability with $V_{DD} = 3\text{ V}$ Figure 12. Source and Sink Current Capability with $V_{DD} = 5\text{ V}$ 

Figure 13. Supply Current vs. Code

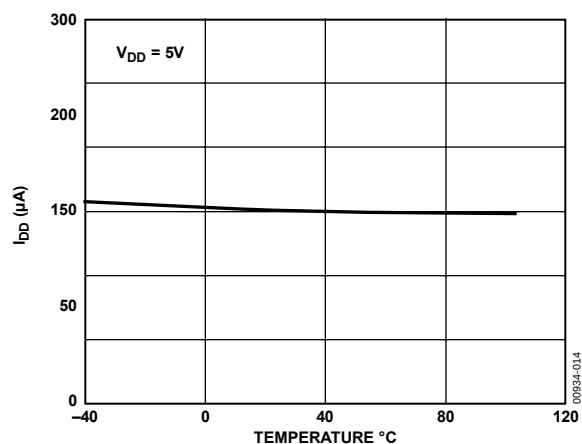


Figure 14. Supply Current vs. Temperature

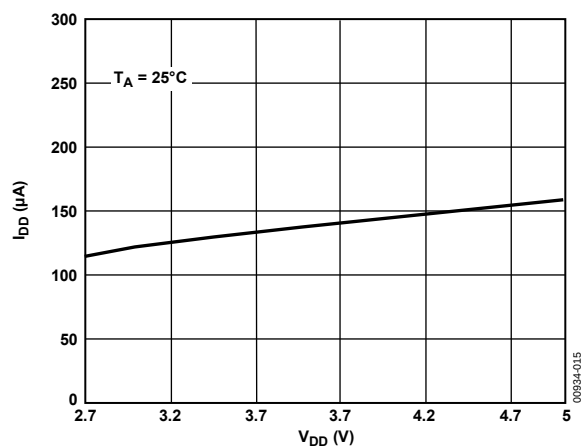


Figure 15. Supply Current vs. Supply Voltage

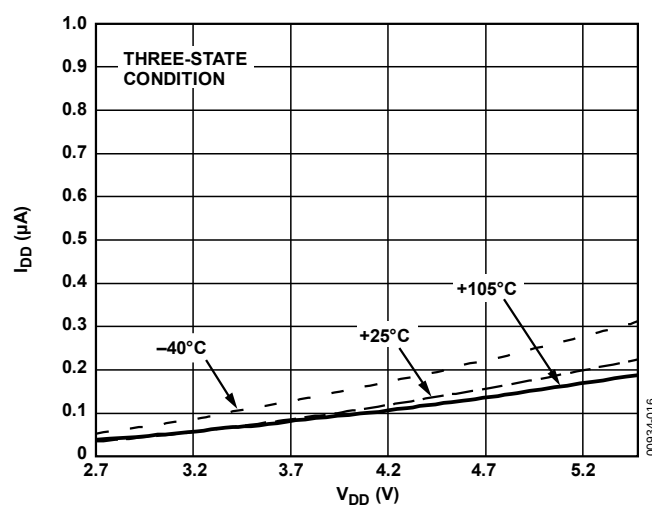


Figure 16. Power-Down Current vs. Supply Voltage

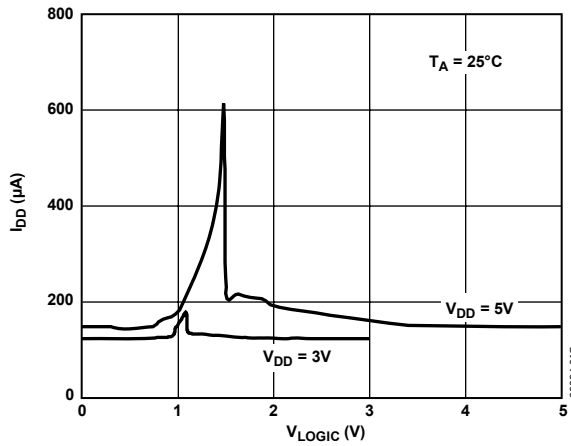
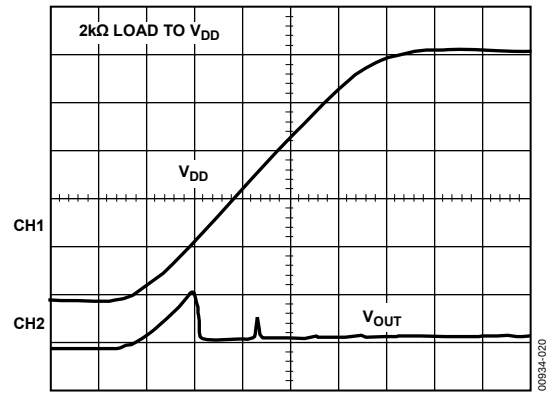
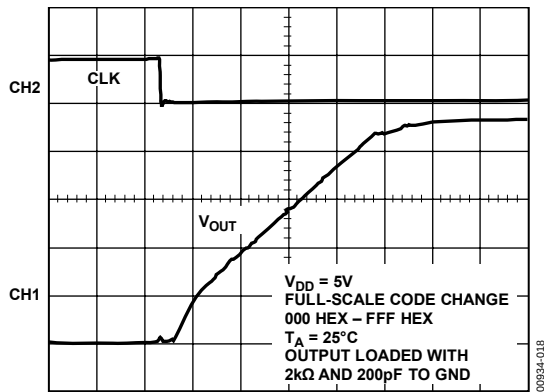


Figure 17. Supply Current vs. Logic Input Voltage



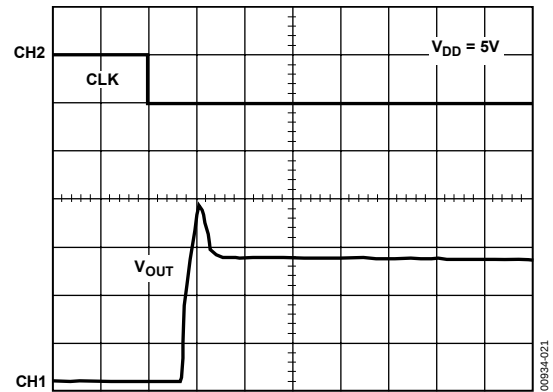
CH1 1V, CH2 1V, TIME BASE = $20\mu s/DIV$

Figure 20. Power-On Reset to 0 V



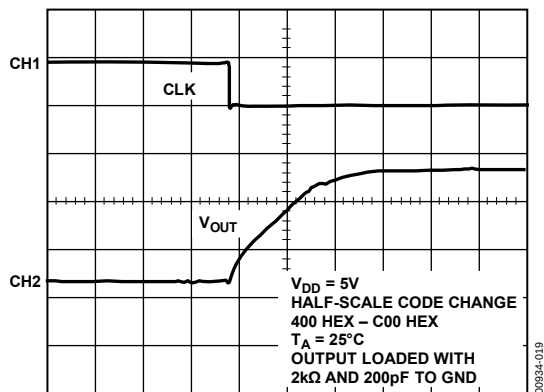
CH1 1V, CH2 5V, TIME BASE = $1\mu s/DIV$

Figure 18. Full-Scale Settling Time



CH1 1V, CH2 5V, TIME BASE = $5\mu s/DIV$

Figure 21. Exiting Power-Down (800 Hex Loaded)



CH1 1V, CH2 5V, TIME BASE = $1\mu s/DIV$

Figure 19. Half-Scale Settling Time

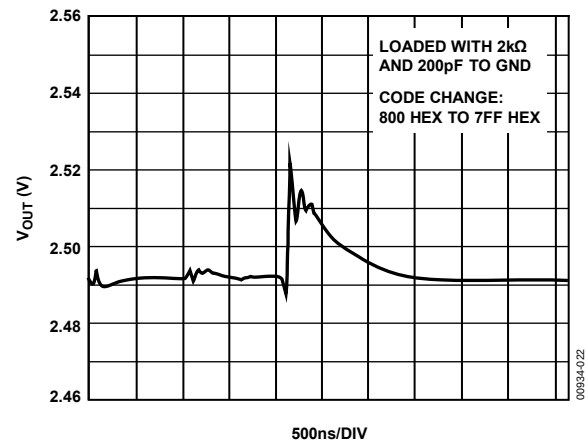


Figure 22. Digital-to-Analog Glitch Impulse

THEORY OF OPERATION

D/A SECTION

The AD5320 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Because there is no reference input pin, the power supply (V_{DD}) acts as the reference. Figure 23 shows a block diagram of the DAC architecture.

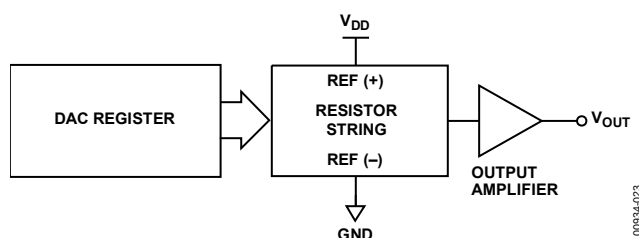


Figure 23. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{DD} \times \left(\frac{D}{4096} \right)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095.

RESISTOR STRING

The resistor string section is shown in Figure 24. It is simply a string of resistors, each of value R . The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

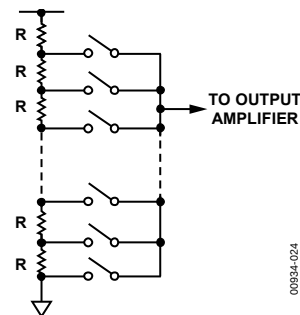


Figure 24. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output that gives an output range of 0 V to V_{DD} . It is capable of driving a load of 2 k Ω in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 11 and Figure 12. The slew rate is 1 V/ μ s with a half-scale settling time of 8 μ s with the output unloaded.

SERIAL INTERFACE

The AD5320 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN) that is compatible with SPI®, QSPI™, and MICROWIRE™ interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the DIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5320 compatible with high speed DSPs. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{\text{SYNC}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Because the $\overline{\text{SYNC}}$ buffer draws more current when $V_{\text{IN}} = 2.4 \text{ V}$ than it does when $V_{\text{IN}} = 0.8 \text{ V}$, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part. As previously mentioned, $\overline{\text{SYNC}}$ must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 25). The first two bits are “don’t cares.” The next two are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next twelve bits are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK.

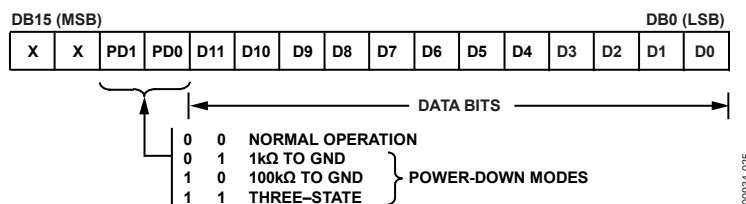


Figure 25. Input Register Contents

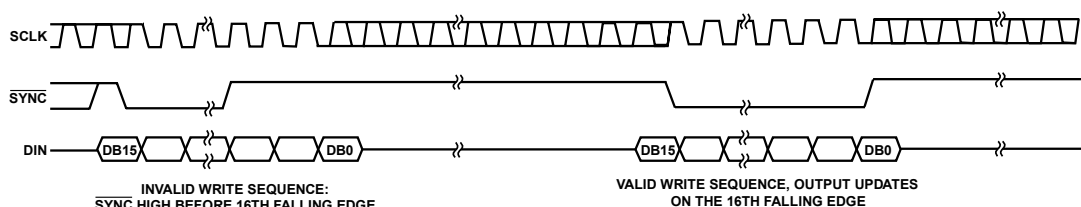


Figure 26. $\overline{\text{SYNC}}$ Interrupt Facility

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, then this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 26).

POWER-ON RESET

The AD5320 contains a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The AD5320 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB13 and DB12) in the control register. Table 5 shows how the state of the bits corresponds to the mode of operation of the device.

Table 5. Modes of Operation for the AD5320

DB13	DB12	Operating Mode
0	0	Normal Operation
		Power-Down Modes
0	1	1 k Ω to GND
1	0	100 k Ω to GND
1	1	Three-State

When both bits are set to 0, the part works with its normal power consumption of 140 μ A at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND through a 1 k Ω resistor, the output is connected internally to GND through a 100 k Ω resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 27.

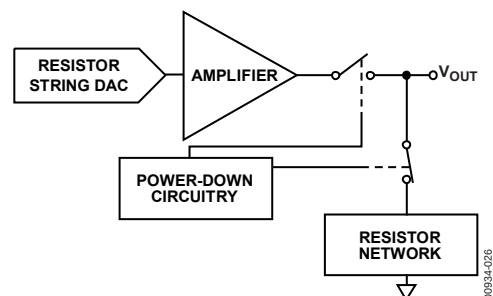


Figure 27. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μ s for $V_{DD} = 5$ V and 5 μ s for $V_{DD} = 3$ V (see Figure 21).

MICROPROCESSOR INTERFACING

AD5320 TO ADSP-2101/ADSP-2103 INTERFACE

Figure 28 shows a serial interface between the AD5320 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in the serial port (SPORT) transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

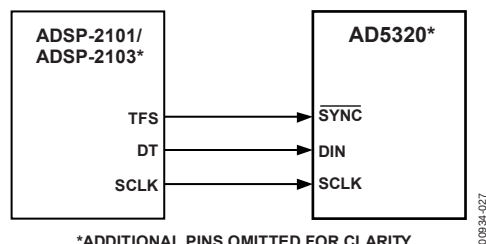


Figure 28. AD5320 to ADSP-2101/ADSP-2103 Interface

AD5320 TO 68HC11/68L11 INTERFACE

Figure 29 shows a serial interface between the AD5320 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5320, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7). For correct operation of this interface, the 68HC11/68L11 should be configured so that the CPOL bit is a 0 and the CPHA bit is a 1. When data is being transmitted to the DAC, the SYNC line is taken low (PC7). When the 68HC11/68L11 are configured, data appearing on the MOSI output is valid on the falling edge of SCK as shown in Figure 29.

Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5320, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken high at the end of this procedure.

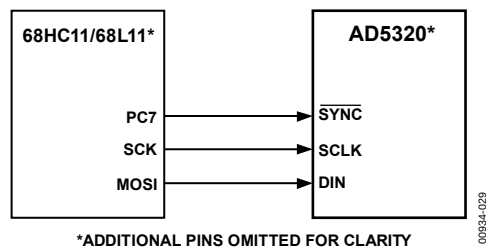


Figure 29. AD5320 to 68HC11/68L11 Interface

AD5320 TO 80C51/80L51 INTERFACE

Figure 30 shows a serial interface between the AD5320 and the 80C51/80L51 microcontrollers. TXD of the 80C51/80L51 drives SCLK of the AD5320, while RXD drives the serial data line of the part. The SYNC signal is again derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the AD5320, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5320 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should consider this.

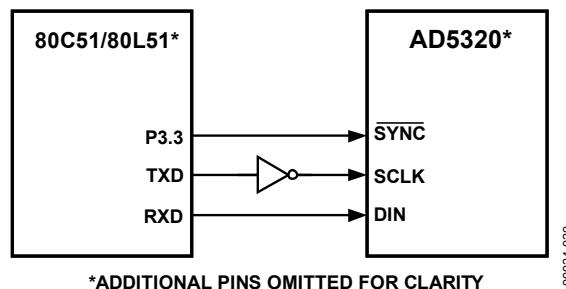


Figure 30. AD5320 to 80C51/80L51 Interface

AD5320 TO MICROWIRE INTERFACE

Figure 31 shows an interface between the AD5320 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5320 on the rising edge of the SK.

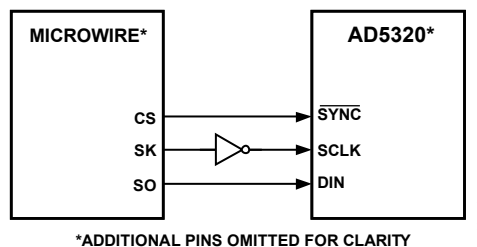


Figure 31. AD5320 to MICROWIRE Interface

APPLICATIONS

USING REF19X AS A POWER SUPPLY FOR AD5320

Because the supply current required by the AD5320 is extremely low, an alternative option is to use a REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) to supply the required voltage to the part (see Figure 32). This is especially useful if the power supply is noisy or if the system supply voltages are at some value other than 5 V or 3 V (such as 15 V). The REF19x outputs a steady supply voltage for the AD5320. If the low dropout REF195 is used, the current it needs to supply to the AD5320 is 140 μ A. This is with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 k Ω load on the DAC output) is:

$$140 \mu\text{A} + (5 \text{ V} / 5 \text{ k}\Omega) = 1.14 \text{ mA}$$

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 2.3 ppm (11.5 μ V) for the 1.14 mA current drawn from it. This corresponds to a 0.009 LSB error.

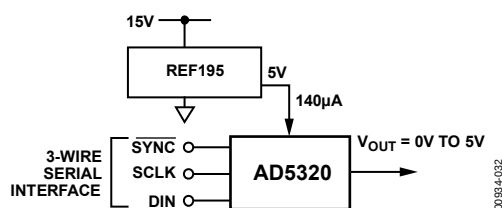


Figure 32. REF195 as Power Supply to AD5320

BIPOLAR OPERATION USING THE AD5320

The AD5320 is designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 33. The circuit below gives an output voltage range of ± 5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{4096} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 4095).

With $V_{DD} = 5$ V, $R1 = R2 = 10$ k Ω :

$$V_O = \left(\frac{10 \times D}{4096} \right) - 5 \text{ V}$$

This is an output voltage range of ± 5 V with 000 hex corresponding to a -5 V output and FFF hex corresponding to a $+5$ V output.

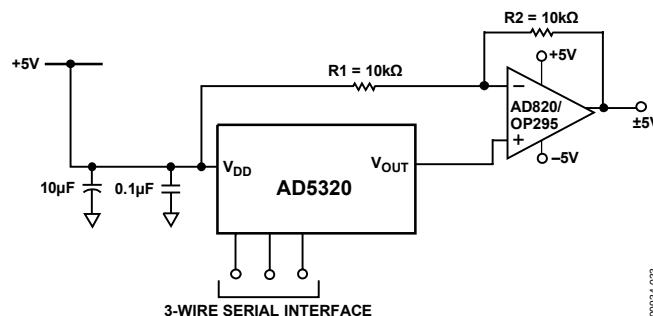


Figure 33. Bipolar Operation with the AD5320

USING AD5320 WITH AN OPTO-ISOLATED INTERFACE

For process control applications in industrial environments, it is often necessary to use an opto-isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. Opto-isolators provide isolation in excess of 3 kV. Because the AD5320 uses a 3-wire serial logic interface, it requires only three opto-isolators to provide the required isolation (see Figure 34). The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5320.

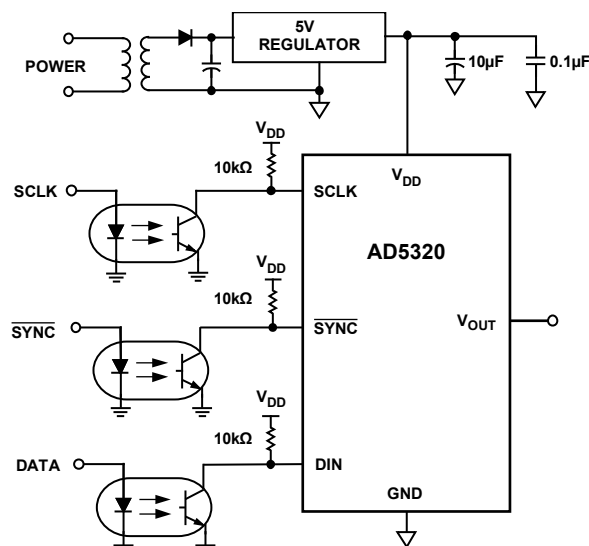


Figure 34. AD5320 with An Opto-Isolated Interface

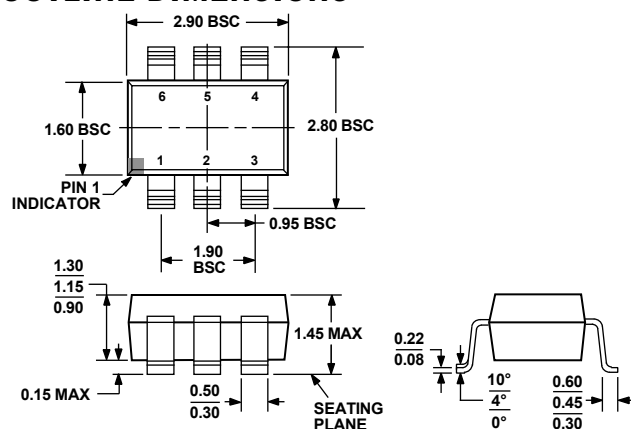
POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to consider carefully the power supply and ground return layout on the board. The printed circuit board containing the AD5320 should have separate analog and digital sections, each having its own area of the board. If the AD5320 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5320.

The power supply to the AD5320 should be bypassed with 10 μF capacitors and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device with the 0.1 μF capacitors ideally against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitors have low effective series resistance (ESR) and effective series inductance (ESI), such as common ceramic types of capacitors. The 0.1 μF capacitors provide a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a two-layer board.

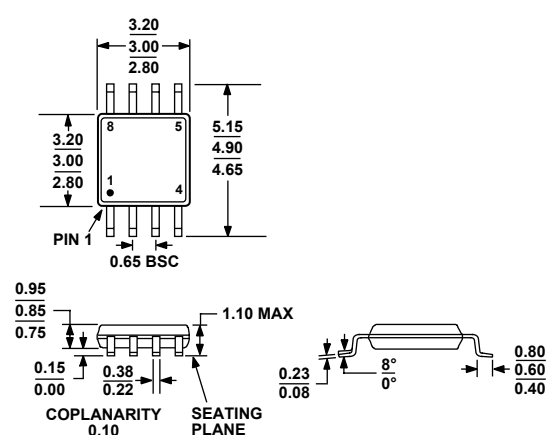
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 35. 6-Lead Small Outline Transistor Package [SOT-23]
(RT-6)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Branding	Package Option
AD5320BRM	−40°C to +105°C	8-Lead Mini Small Outline Package [MSOP]	D4B	RM-8
AD5320BRM-REEL	−40°C to +105°C	8-Lead Mini Small Outline Package [MSOP]	D4B	RM-8
AD5320BRM-REEL7	−40°C to +105°C	8-Lead Mini Small Outline Package [MSOP]	D4B	RM-8
AD5320BRMZ ¹	−40°C to +105°C	8-Lead Mini Small Outline Package [MSOP]	D9N	RM-8
AD5320BRMZ-REEL ¹	−40°C to +105°C	8-Lead Mini Small Outline Package [MSOP]	D9N	RM-8
AD5320BRMZ-REEL7 ¹	−40°C to +105°C	8-Lead Mini Small Outline Package [MSOP]	D9N	RM-8
AD5320BRT-500RL7	−40°C to +105°C	6-Lead Small Outline Transistor Package [SOT-23]	D4B	RT-6
AD5320BRT-REEL	−40°C to +105°C	6-Lead Small Outline Transistor Package [SOT-23]	D4B	RT-6
AD5320BRT-REEL7	−40°C to +105°C	6-Lead Small Outline Transistor Package [SOT-23]	D4B	RT-6
AD5320BRTZ-500RL7 ¹	−40°C to +105°C	6-Lead Small Outline Transistor Package [SOT-23]	D9N	RT-6
AD5320BRTZ-REEL ¹	−40°C to +105°C	6-Lead Small Outline Transistor Package [SOT-23]	D9N	RT-6
AD5320BRTZ-REEL7 ¹	−40°C to +105°C	6-Lead Small Outline Transistor Package [SOT-23]	D9N	RT-6

¹ Z = Pb-free part.

AD5320

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AD5320

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