Thyristor/Thyristor, 160 A (INT-A-PAK Power Modules)

INT-A-PAK

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	160 A
Type	Modules - thyristor, standard
Package	INT-A-PAK

FEATURES

- High voltage
- Electrically isolated by DBC ceramic (Al_2O_3)
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- High surge capability
- Glass passivated chips
- Modules uses high voltage power thyristor/diodes in three basic configurations
- Simple mounting
- UL approved file E78996
- Designed and qualified for multiple level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT

APPLICATIONS

- DC motor control and drives
- Battery charges
- Welders
- Power converters
- Lighting control
- Heat and temperature control

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$	85 °C	160	A
$I_{T(RMS)}$		355	
I_{TSM}	50 Hz	4870	
	60 Hz	5100	
I^2t	50 Hz	119	kA^2s
	60 Hz	108	
$I^2\sqrt{t}$		1190	$kA^2\sqrt{s}$
V_{RRM}	Range	1200, 1600	V
T_J	Range	-40 to +125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125 °C mA
VS-VSK.162	12	1200	1300	50
	16	1600	1700	

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			160	A
					85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch			355	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial T_J = T_J maximum	4870	
		t = 8.3 ms			5100	
		t = 10 ms	100 % V_{RRM} reapplied		4100	
		t = 8.3 ms			4300	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		119	kA^2s
		t = 8.3 ms			108	
		t = 10 ms	100 % V_{RRM} reapplied		84	
		t = 8.3 ms			76.7	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			1190	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)} < I < \pi$ x $I_{T(AV)}$), T_J maximum			0.8	V
High level value of threshold voltage	$V_{T(TO)2}$	($I > \pi$ x $I_{T(AV)}$), T_J maximum			0.98	
Low level value on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)} < I < \pi$ x $I_{T(AV)}$), T_J maximum			1.67	mΩ
High level value on-state slope resistance	r_{t2}	($I > \pi$ x $I_{T(AV)}$), T_J maximum			1.38	
Maximum on-state voltage drop	V_{TM}	$I_{TM} = \pi$ x $I_{T(AV)}$, T_J = 25 °C, 180° conduction			1.54	V
Maximum forward voltage drop	V_{FM}	$I_{TM} = \pi$ x $I_{T(AV)}$, T_J = 25 °C, 180° conduction			1.54	V
Maximum holding current	I_H	Anode supply = 6 V initial I_T = 30 A, T_J = 25 °C			200	mA
Maximum latching current	I_L	Anode supply = 6 V resistive load = 1 Ω Gate pulse: 10 V, 100 μs, T_J = 25 °C			400	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	t_{gd}	T_J = 25 °C	Gate current = 1 A, dI_g/dt = 1 A/μs V_d = 0.67 % V_{DRM}	1	μs
Typical rise time	t_{gr}			2	
Typical turn-off time	t_q	I_{TM} = 300 A, - dI/dt = 15 A/μs; T_J = T_J maximum V_R = 50 V; dV/dt = 20 V/μs; gate 0 V, 100 Ω		50 to 200	

BLOCKING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	T_J = 125 °C	50	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted, t = 1 s	3500	V
Critical rate of rise of off-state voltage	dV/dt	T_J = T_J maximum, exponential to 67 % rated V_{DRM}	1000	V/μs

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		12	W
Maximum average gate power	$P_{G(AV)}$	f = 50 Hz, $T_J = T_J$ maximum		3	
Maximum peak gate current	I_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		3	A
Maximum peak negative gate voltage	$- V_{GT}$			10	V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = - 40 °C	Anode supply = 6 V, resistive load; $R_a = 1\ \Omega$	4	
		T_J = 25 °C		2.5	
		$T_J = T_J$ maximum		1.7	
Maximum required DC gate current to trigger	I_{GT}	T_J = - 40 °C		270	mA
		T_J = 25 °C		150	
		$T_J = T_J$ maximum		80	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied		0.3	V
Maximum gate current that will not trigger	I_{GD}			10	mA
Maximum rate of rise of turned-on current	dI/dt	$T_J = T_J$ maximum, I_{TM} = 400 A rated V_{DRM} applied		300	A/μs

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range		T_J		-40 to +125	°C
Maximum storage temperature range		T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case per junction		R_{thJC}	DC operation	0.16	K/W
Maximum thermal resistance, case to heat sink per module		R_{thCS}	Mounting surface, smooth, flat and greased	0.05	
Mounting torque ± 10 %	IAP to heat sink		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6	Nm
	busbar to IAP				
Approximate weight				200	g
				7.1	oz.
Case style				INT-A-PAK	

ΔR CONDUCTION PER JUNCTION

DEVICES	SINUSOIDAL CONDUCTION AT T_J MAXIMUM					RECTANGULAR CONDUCTION AT T_J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-VSK.162	0.0030	0.0031	0.0032	0.0033	0.0034	0.0029	0.0036	0.0039	0.0041	0.0040	K/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

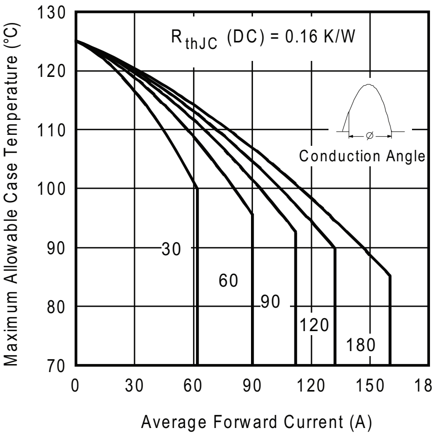


Fig. 1 - Current Ratings Characteristics

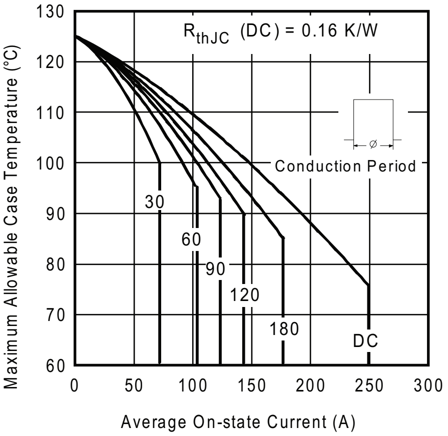


Fig. 2 - Current Ratings Characteristics

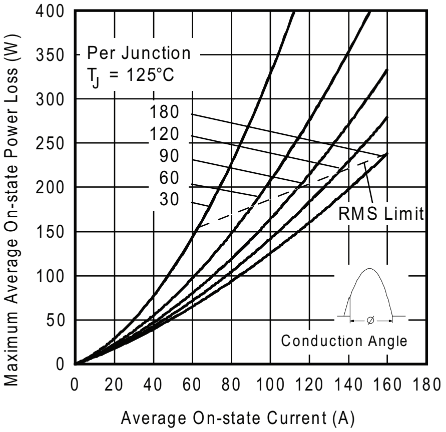


Fig. 3 - On-State Power Loss Characteristics

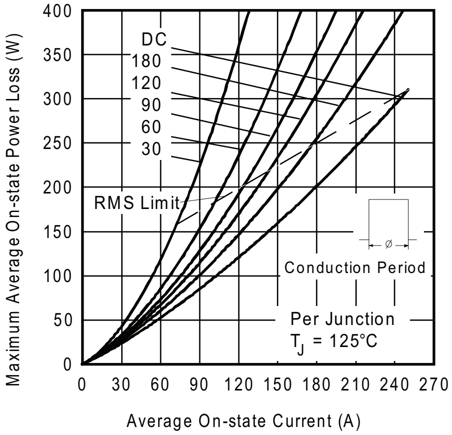


Fig. 4 - On-State Power Loss Characteristics

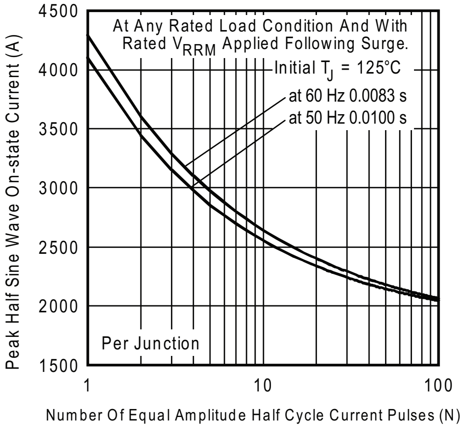


Fig. 5 - Maximum Non-Repetitive Surge Current

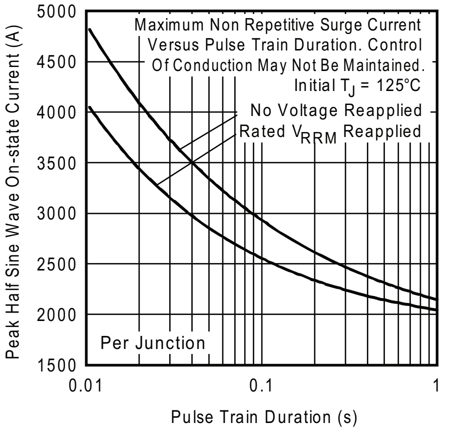


Fig. 6 - Maximum Non-Repetitive Surge Current

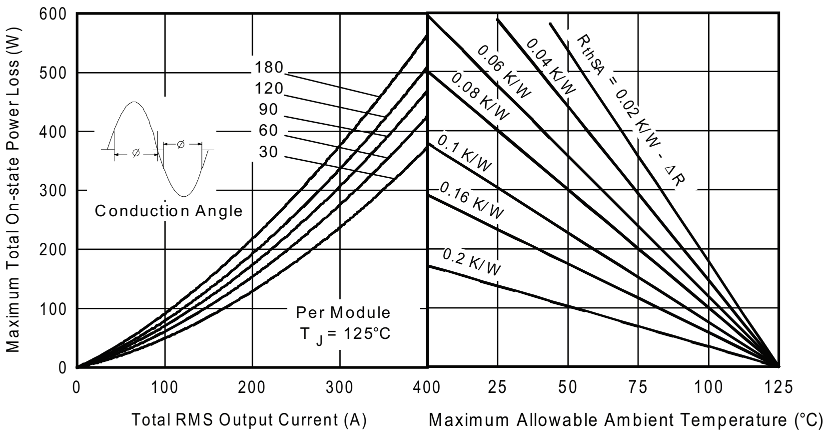


Fig. 7 - On-State Power Loss Characteristics

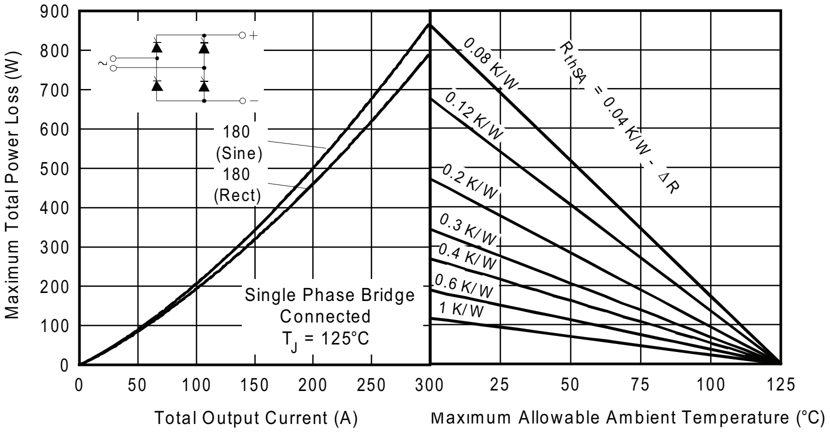


Fig. 8 - On-State Power Loss Characteristics

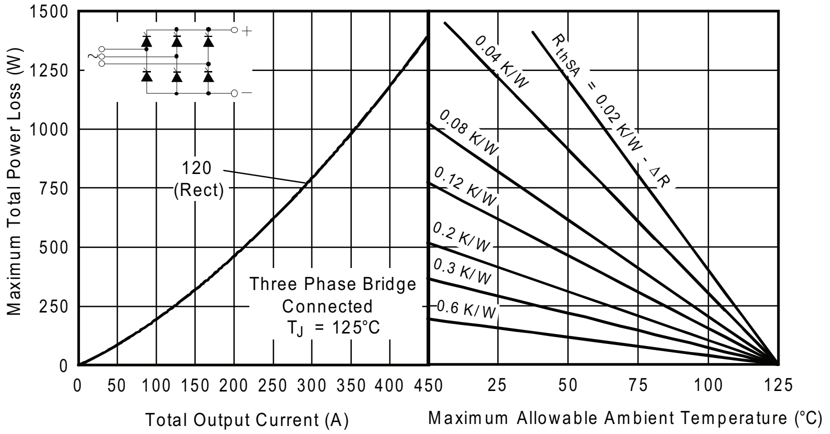


Fig. 9 - On-State Power Loss Characteristics

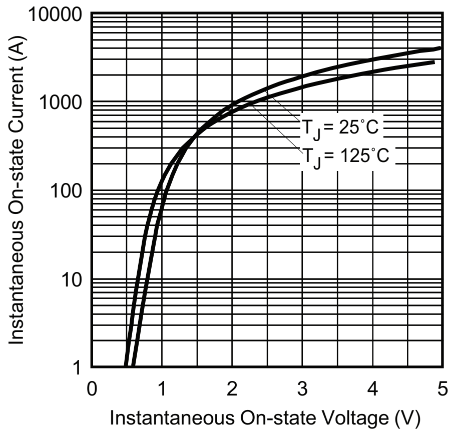


Fig. 10 - On-State Voltage Drop Characteristics

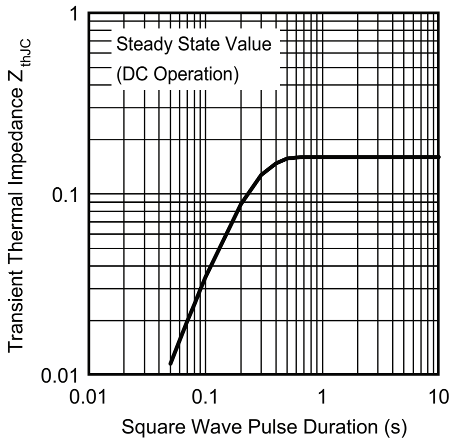


Fig. 11 - Thermal Impedance Z_{thJC} Characteristics

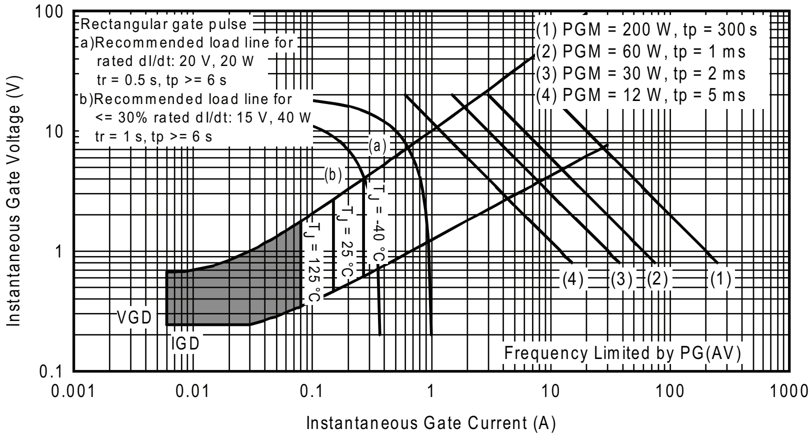


Fig. 12 - Gate Characteristics

ORDERING INFORMATION TABLE

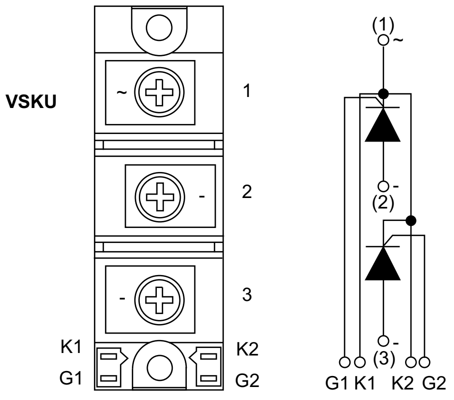
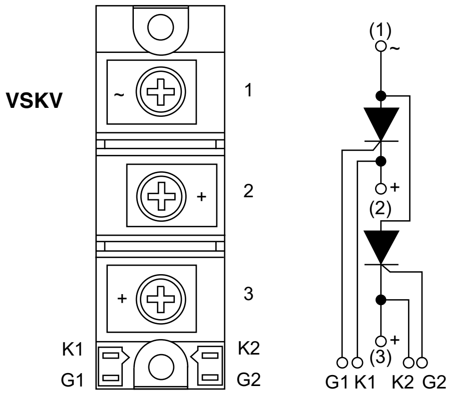
Device code	VS-VS	KU	162	16	PbF
	①	②	③	④	⑤

1	-	Vishay Semiconductors product
2	-	Circuit configuration
3	-	Current rating: $I_{T(AV)}$
4	-	Voltage code x 100 = V_{RRM}
5	-	PbF = Lead (Pb)-free

Note

- To order the optional hardware go to www.vishay.com/doc?95172

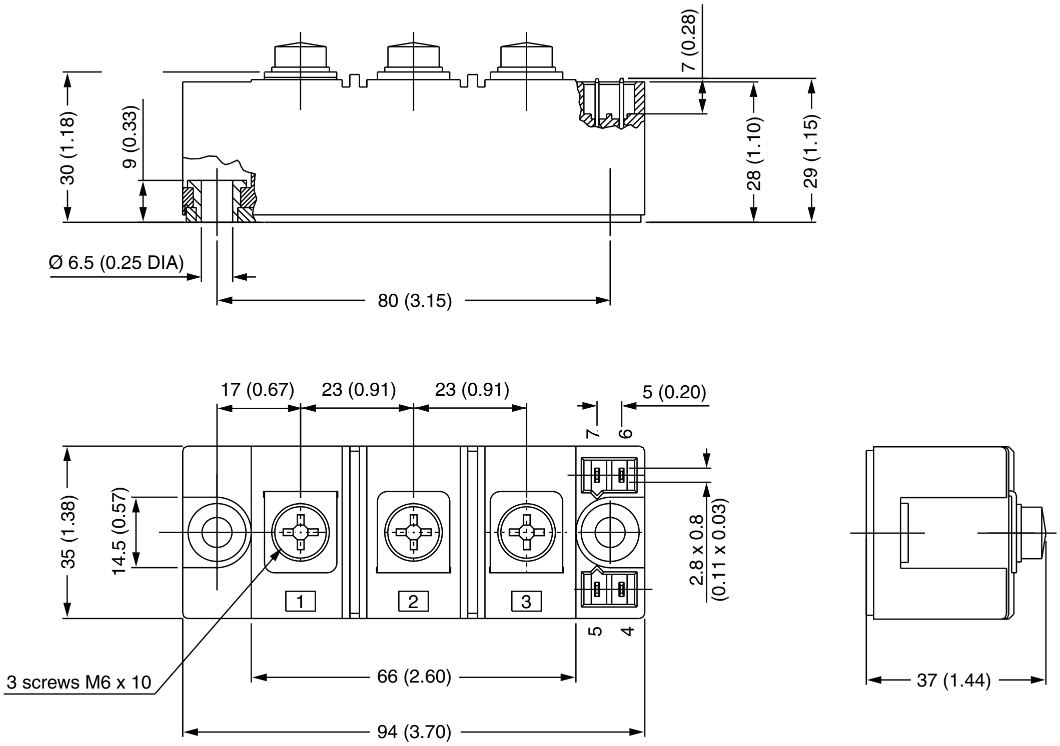
CIRCUIT CONFIGURATION

CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs common cathodes	U	
Two SCRs common anodes	V	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95067

INT-A-PAK IGBT/Thyristor

DIMENSIONS in millimeters (inches)



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