

74AHC541-Q100; 74AHCT541-Q100

Octal buffer/line driver; 3-state

Rev. 2 — 14 April 2020

Product data sheet

1. General description

The 74AHC541-Q100; 74AHCT541-Q100 is a high-speed Si-gate CMOS device.

The 74AHC541-Q100; 74AHCT541-Q100 are octal non-inverting buffer/line drivers with 3-state bus compatible outputs.

The output enable inputs $\overline{OE}0$ and $\overline{OE}1$, control the 3-state outputs.

A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accept voltages higher than V_{CC}
- For 74AHC541-Q100 only: operates with CMOS input levels
- For 74AHCT541-Q100 only: operates with TTL input levels
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC541D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT541D-Q100				
74AHC541PW-Q100	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74AHCT541PW-Q100				
74AHC541BQ-Q100	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74AHCT541BQ-Q100				

4. Functional diagram



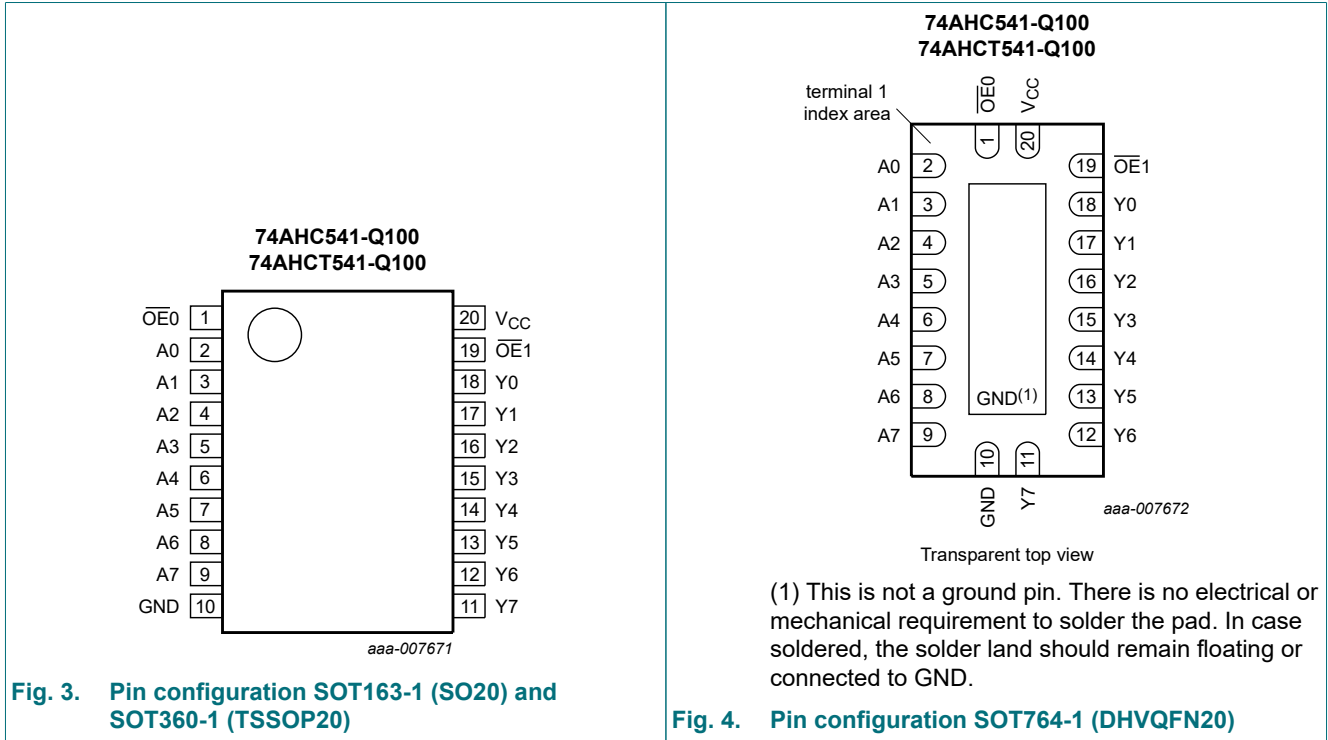
Fig. 1. Logic symbol



Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}0$	1	output enable input (active LOW)
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{OE}1$	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control		Input	Output
$\overline{OE}0$	$\overline{OE}1$	A _n	Y _n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	± 20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	± 25	mA
I_{CC}	supply current		-	75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
 For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
 For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC541-Q100			74AHCT541-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V \pm 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V \pm 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC541-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V		
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C _I	input capacitance		-	3.0	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHCT541-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; I _O = 0 A; V _O = V _{CC} or GND; other pins at V _{CC} or GND	-	-	±0.25	-	±2.5	-	±10.0	µA
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other pins at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$. For test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
For type 74AHC541-Q100										
t_{pd}	propagation delay	An to Yn; see Fig. 5 [2]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	5.0	7.0	1.0	8.5	1.0	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	7.0	10.5	1.0	12.0	1.0	13.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.5	5.0	1.0	6.0	1.0	6.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$		5.0	7.0	1.0	8.0	1.0	9.0	ns
t_{en}	enable time	$\overline{O}E_n$ to Yn; see Fig. 6 [2]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	5.5	10.5	1.0	11.0	1.0	13.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	7.5	14.0	1.0	16.0	1.0	17.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.5	7.2	1.0	8.5	1.0	9.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.0	9.2	1.0	10.5	1.0	11.5	ns
t_{dis}	disable time	$\overline{O}E_n$ to Yn; see Fig. 6 [2]								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 15\text{ pF}$	-	6.0	11.0	1.0	12.0	1.0	14.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}; C_L = 50\text{ pF}$	-	9.5	15.4	1.0	17.5	1.0	19.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	4.5	7.5	1.0	8.0	1.0	9.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	6.5	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	$C_L = 50\text{ pF}; f_i = 1\text{ MHz}; V_i = GND\text{ to }V_{CC}$ [3]	-	10	-	-	-	-	-	pF
For type 74AHCT541-Q100										
t_{pd}	propagation delay	An to Yn; see Fig. 5 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	3.5	5.5	1.0	6.5	1.0	7.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.0	8.5	1.0	9.5	1.0	11.0	ns
t_{en}	enable time	$\overline{O}E_n$ to Yn; see Fig. 6								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	4.0	7.0	1.0	8.0	1.0	9.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	5.5	10.0	1.0	12.0	1.0	12.5	ns
t_{dis}	disable time	$\overline{O}E_n$ to Yn; see Fig. 6 [2]								
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 15\text{ pF}$	-	5.0	7.0	1.0	8.0	1.0	9.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}; C_L = 50\text{ pF}$	-	7.0	10.0	1.0	12.0	1.0	12.5	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50\text{ pF}; f = 1\text{ MHz}; V_i = GND\text{ to }V_{CC}$ [3]	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3\text{ V}$ and $V_{CC} = 5.0\text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{en} is the same as t_{PZL} and t_{PZH} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

10.1. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Propagation delay input (An) to output (Yn)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC541-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
74AHCT541-Q100	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC541-Q100	V_{CC}	3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT541-Q100	3.0 V	3.0 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

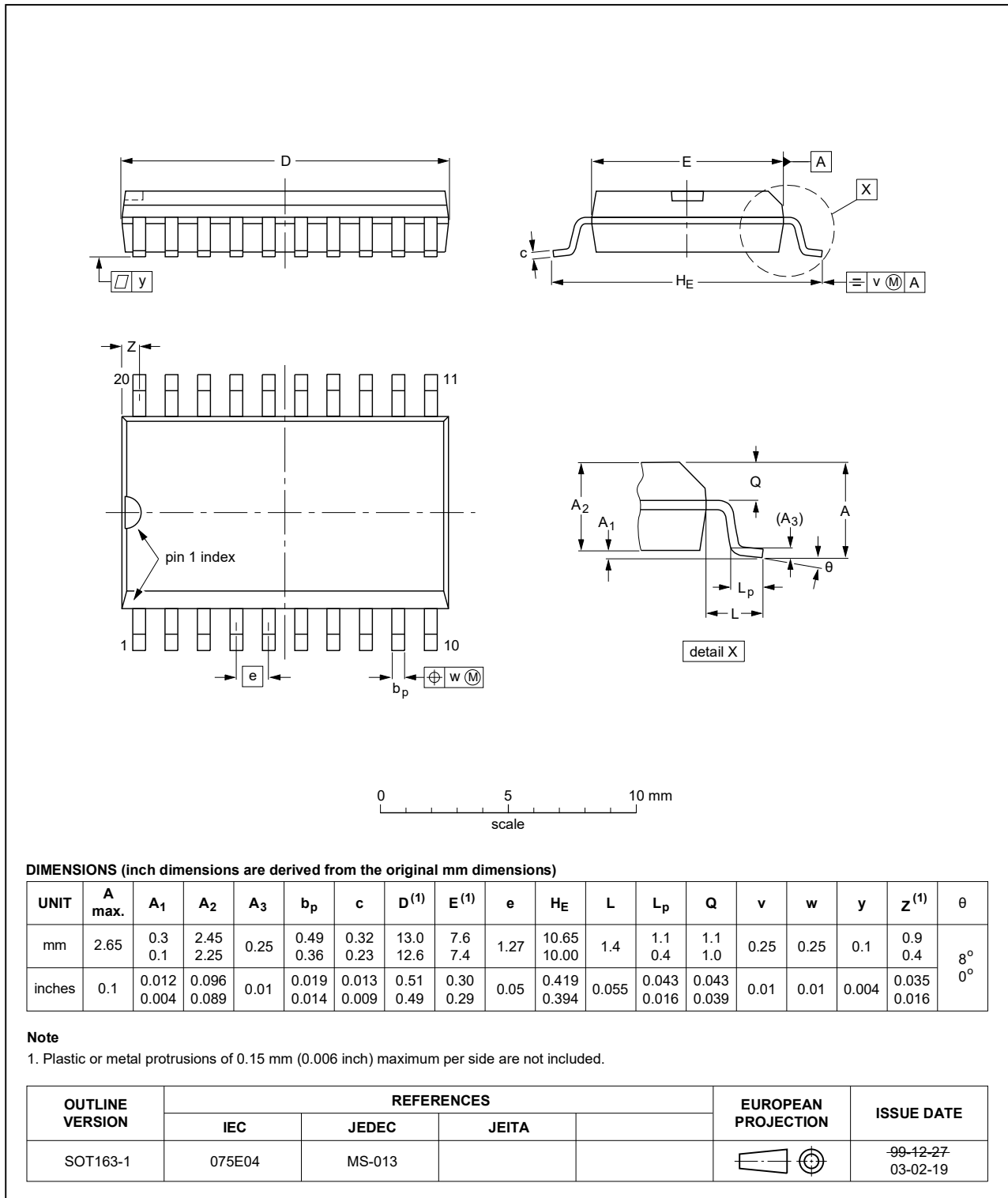


Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 10. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT541_Q100 v.2	20200414	Product data sheet	-	74AHC_AHCT541_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 10: Package outline drawing SOT764-1 (DHVQFN20) updated. 			
74AHC_AHCT541_Q100 v.1	20130606	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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