TEMPERATURE SWITCH IC WITH LATCH S-5840B Series

The temperature switch IC S-5840B Series with a latch function detects temperature with the accuracy of ±2.5°C. When the temperature reaches the detection temperature, the output signal is inverted and being latched until this IC detects decrease in a power supply voltage.
The minimum power supply voltage is 1.0 V which is required to operate this IC, the current consumption is as low as 12 μA (typ.) due to CMOS configuration. The S-5840B Series has a temperature sensor using negative temperature coefficient, a reference voltage source, comparator, voltage detection circuit and noise suppression circuit on a chip, and they are enclosed in package SOT-23-5.
Since the temperature range of this IC is –40 to +100°C, it is possible to achieve the extensive application for temperature control.

■ Features

- Detection temperature : +55 to +95°C, 1°C step, detection accuracy : ±2.5°C
- Wide voltage range during operation : V_{DD} = 1.0 to 10.0 V
- Release voltage : 2.2 to 3.4 V, 0.1 V step
- Low current consumption : 12 μA typ. (+25°C)
- Built-in circuit for preventing temperature detection malfunction
- Output logic level is fixed by the latch after temperature detection
- Output logic active high or active low is selectable
- Output CMOS or Nch open drain is selectable
- Package : SOT-23-5
- Lead-free product

■ Applications

- Game consoles
- Electronic devices

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
SOT-23-5	MP005-A	MP005-A	MP005-A

■ Block Diagram

1. S-5840B with CMOS output

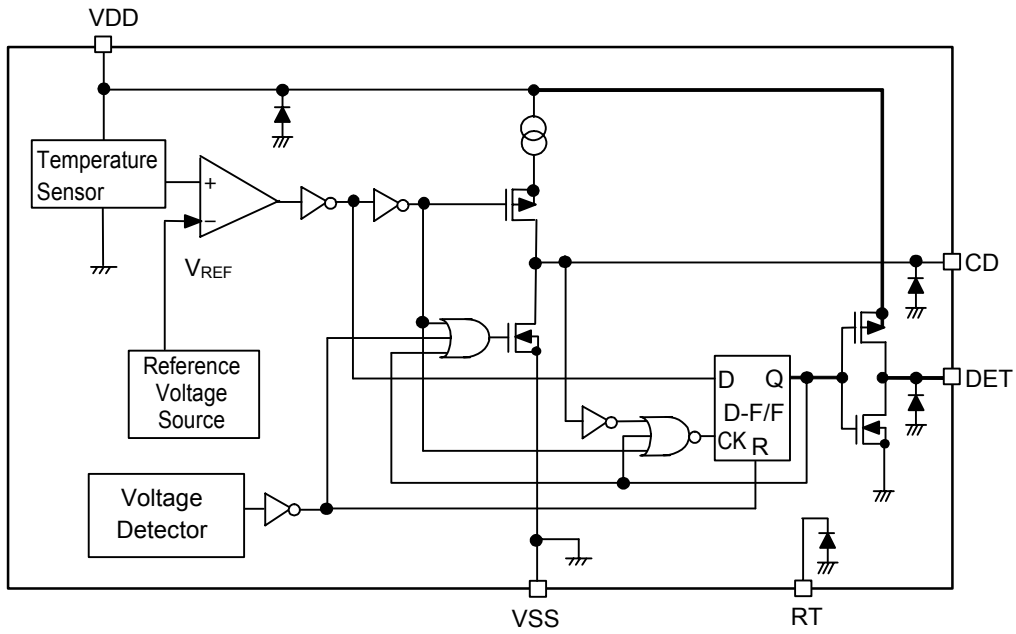


Figure 1

2. S-5840B with Nch open drain output

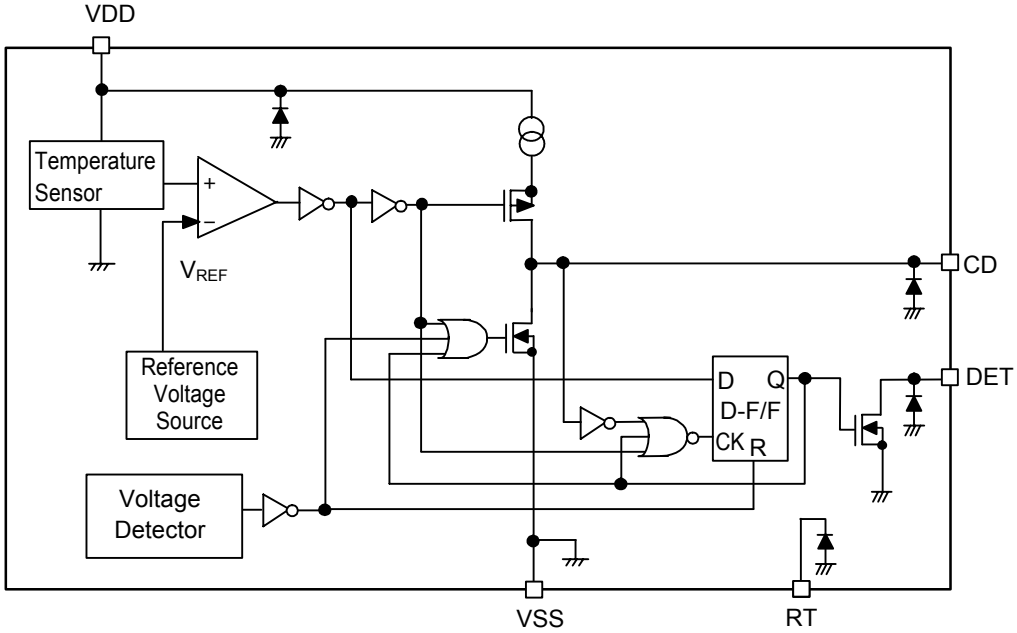
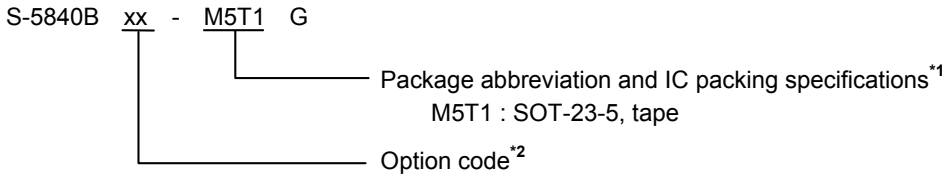


Figure 2

■ Product Name Structure

1. Product name



***1.** Refer to the taping specifications at the end of this booklet.

***2.** Option list

- Detection temperature (T_{DET}) is selectable in 1°C step in the range of 55 to 95°C.
- DET output is selectable in active high or active low.
- DET output is selectable in CMOS or Nch open drain.
- Release voltage (V_{RET}) is selectable in 0.1 V step in the range of 2.2 to 3.4 V.

2. Product name list

Table 1

Product name	Detection temperature (T_{DET})	Output form	Output logic	Release voltage (V_{RET})
S-5840BAG-M5T1G	60°C	CMOS	Active low	2.9 V
S-5840BAH-M5T1G	90°C	CMOS	Active high	2.9 V
S-5840BAJ-M5T1G	80°C	Nch open drain	Active low	2.2 V

Remark Please contact our sales office for options other than that specified above.

■ Pin Configuration

SOT-23-5
Top view

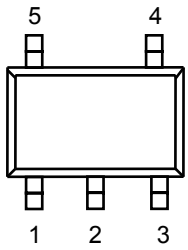


Figure 3

Table 2

Pin No.	Symbol	Description
1	RT *1	Test pin
2	VSS	GND pin
3	CD	Capacitor connection pin for setting malfunction prevention time
4	DET	Output pin
5	VDD	Power supply pin

***1.** Set the RT pin open in use.

Remark See Dimensions for details of the package drawings.

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Parameter		Symbol	Rating	Unit
Power supply voltage (V_{SS} = 0 V)		V_{DD}	V_{SS} + 12	V
Pin voltage		V_{RT}, V_{CD}	V_{SS} − 0.3 to V_{DD} + 0.3	V
Output voltage	CMOS output	V_{DET}	V_{SS} − 0.3 to V_{DD} + 0.3	V
	Nch open drain output		V_{SS} − 0.3 to V_{SS} + 12.0	V
Power dissipation		P_D	300 (When not mounted on board)	mW
			600*1	mW
Operating temperature		T_{opr}	−40 to +100	°C
Storage temperature		T_{stg}	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Values for External Parts

Table 4

Parameter	Symbol	Value	Unit
CD capacitance	C_D	4.7	nF

■ DC Electrical Characteristics

1. Product with CMOS output

Table 5

(Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	–		1.0	–	10.0	V
Detection temperature	T_D	–		T_{DET} – 2.5	T_{DET}	T_{DET} + 2.5	°C
Output current	I_{DETH}	V_{DD} = 3.5 V, Apply for DET pin	V_{DET} = 2.7 V	2	9.4	–	mA
	I_{DETL}		V_{DET} = 0.4 V	0.5	2.8	–	mA
Release voltage for built-in voltage detector	V_R	–		V_{RET} × 0.98	V_{RET}	V_{RET} × 1.02	V
Hysteresis width for built-in voltage detector	V_{HYS}	–		–	V_{RET} × 0.05	–	V
Temperature coefficient for built-in voltage detector	$\frac{\Delta V_{RET}}{\Delta Ta \bullet V_{RET}}$	Ta = –40 to +100°C		–	±100	–	ppm/°C
Operating current	I_{DD}	V_{DD} = 3.5 V		–	12	24	μA

2. Product with Nch open drain output

Table 6

(Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	–	1.0	–	10.0	V
Detection temperature	T_D	–	T_{DET} – 2.5	T_{DET}	T_{DET} + 2.5	°C
Output current	I_{DETL}	V_{DET} = 0.4 V, V_{DD} = 3.5 V	0.5	2.8	–	mA
	I_{LEAK}	V_{DET} = 10.0 V, V_{DD} = 3.5 V	–	–	100	nA
Release voltage for built-in voltage detector	V_R	–	V_{RET} × 0.98	V_{RET}	V_{RET} × 1.02	V
Hysteresis width for built-in voltage detector	V_{HYS}	–	–	V_{RET} × 0.05	–	V
Temperature coefficient for built-in voltage detector	$\frac{\Delta V_{RET}}{\Delta Ta \bullet V_{RET}}$	Ta = –40 to +100°C	–	±100	–	ppm/°C
Operating current	I_{DD}	V_{DD} = 3.5 V	–	12	24	μA

■ AC Electrical Characteristics

Table 7

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Noise filtering time	t_{noise}	C_D = 4.7 nF, V_{DD} = 3.5 V, Ta = detection temperature	10	30	50	ms

■ Operation

Basic operation

The S-5840B Series is a temperature switch IC which detects the temperature and sends a signal to an external device. The users can select a combination of the parameters such as detection temperature and release voltage.

The following explains the case when DET output is assumed to be active high.
When the power supply voltage is turned on, the DET pin voltage goes to low since the flip-flop circuit in the detection circuit is cleared by the voltage detection circuit. Temperature detection then starts and the DET pin is held low as long as the temperature is lower than the detection temperature. When the temperature rises and when the temperature exceeds the detection temperature; longer than the time defined by the capacitor connected to the CD pin, the DET pin goes to high. Once the over-temperature is detected and the DET pin goes to high, the state is held by the flip-flop circuit. In order to release the state, the power supply voltage should be set under the detection voltage ($V_R - V_{HYS}$) of the built-in voltage detector circuit to reset the internal circuit.
Using the internal reference voltage and built-in temperature sensor, a detection temperature accuracy of ±2.5°C is achieved in the IC.

[Noise filtering circuit]

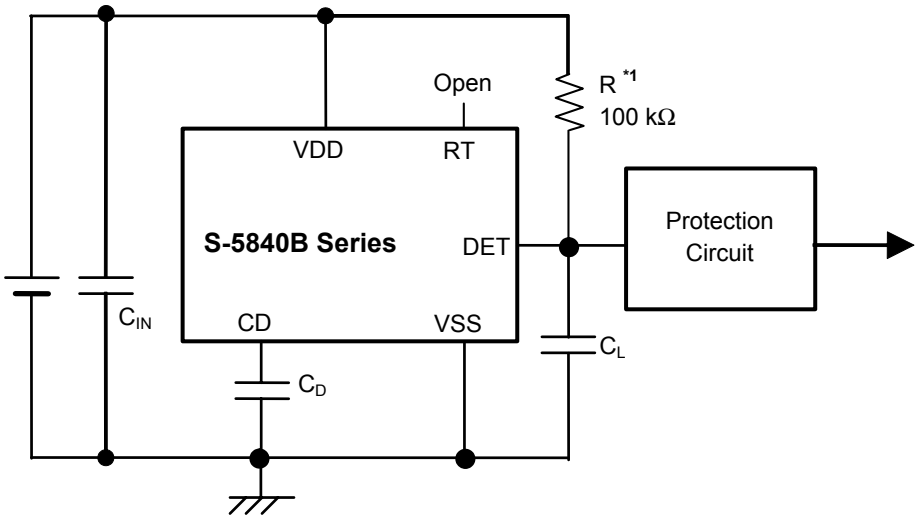
The noise filtering circuit prevents malfunction of the temperature switch caused by noise.
The noise filtering circuit starts charging the capacitor connected to the CD pin when the output of the internal comparator enters the active state due to an external noise or a rapid change in the power supply voltage. In the normal operation, the flip-flop circuit is set when the capacitor is charged to a certain voltage. But in the noise triggered operation, the comparator output goes back to the inactive state and the CD pin voltage is held low since the charging of the capacitor is insufficient. As a result, the DET pin is held low and malfunction does not occur.

Noise filtering time (t_{noise}) is determined by the time constant consisting of internal constant current and the capacitance (C_D), and calculated by the following equation.

t_{noise} (ms) = Noise filtering time coefficient × C_D (nF)
Noise filtering time coefficient (25°C) : Typ. 6.4

Capacitance of the external capacitor C_D has no limitation as long as its leak current is negligible compared to the internal constant current. The difference occurs in delay time if the capacitor has a leak current.

■ Application Circuit



***1.** Connecting a resistor (R) is unnecessary for the product with CMOS output.

Figure 4

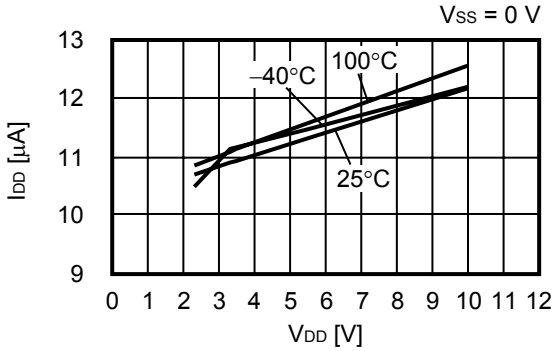
Caution The above connection diagram will not guarantee successful operation. Perform thorough evaluation using actual application to set the constant.

■ Precautions

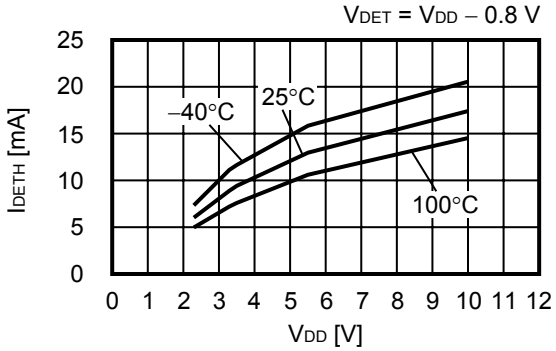
- Set a capacitor (C_{IN}) of about 0.1 μF between VDD and VSS for stabilization.
- A capacitor (C_L) of about 1 μF should be connected to the DET pin to prevent malfunction caused by noise due to the power being on.
- Do not connect a capacitor to the RT pin (leave the RT pin open). Otherwise, this IC may oscillate.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products, including this IC, of patents owned by a third party.

■ Characteristics (Typical Data)

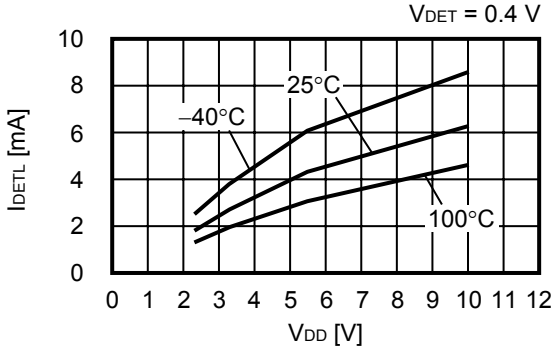
1. Current consumption vs. Power supply voltage characteristics



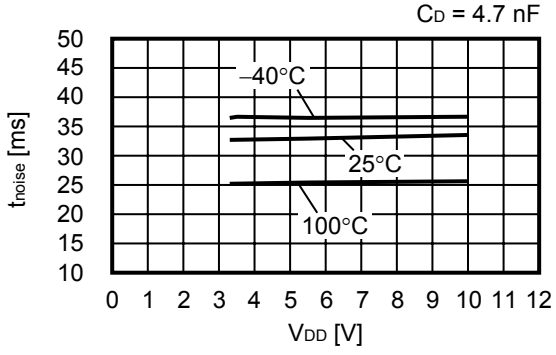
2. DET pin current H vs. Power supply voltage characteristics (product with CMOS output)



3. DET pin current L vs. Power supply voltage characteristics

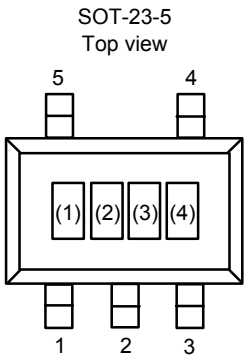


4. Noise filtering time vs. Power supply voltage characteristics



■ Marking Specification

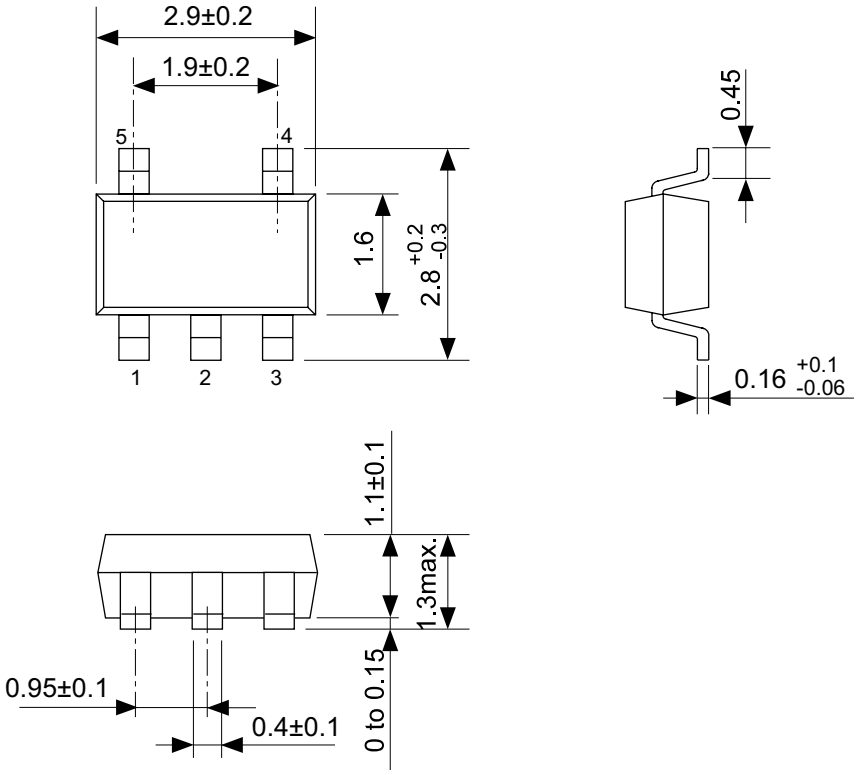
SOT-23-5



(1) to (3) : Product code (refer to **Product name vs. Product code**)
(4) : Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-5840BAG-M5T1G	H	8	M
S-5840BAH-M5T1G	H	8	N
S-5840BAJ-M5T1G	H	8	O



No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
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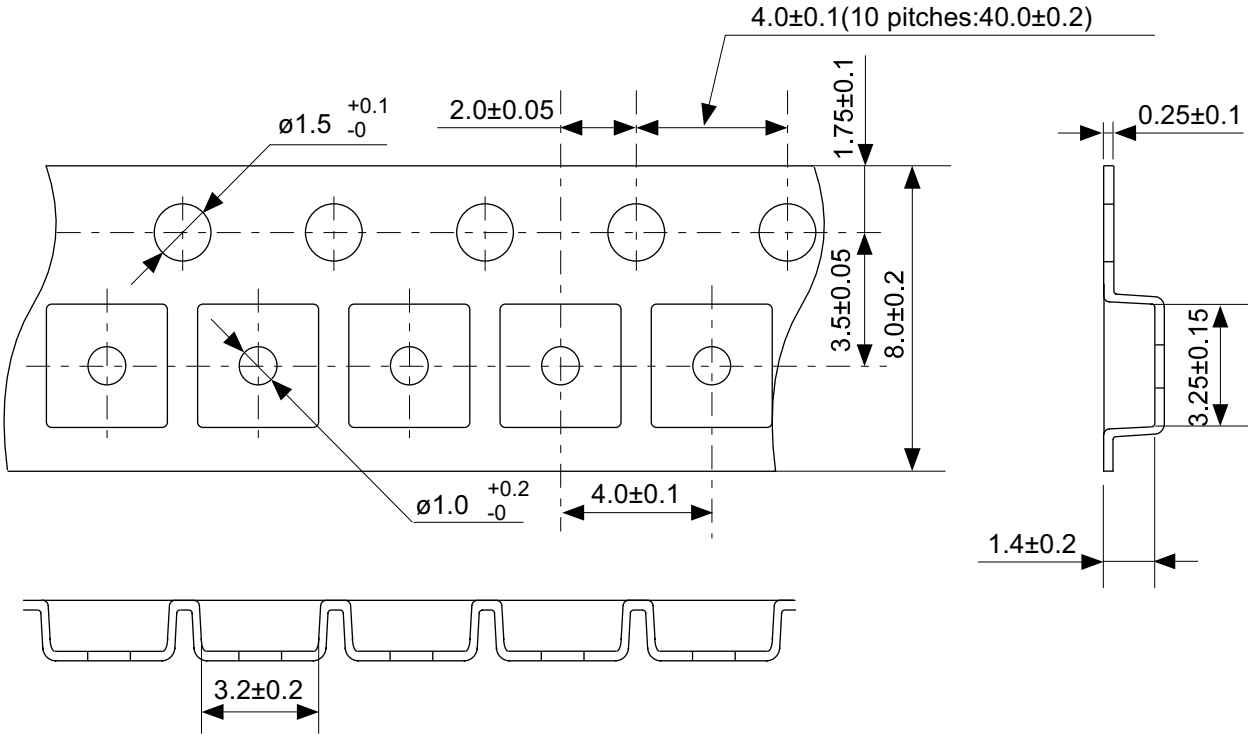
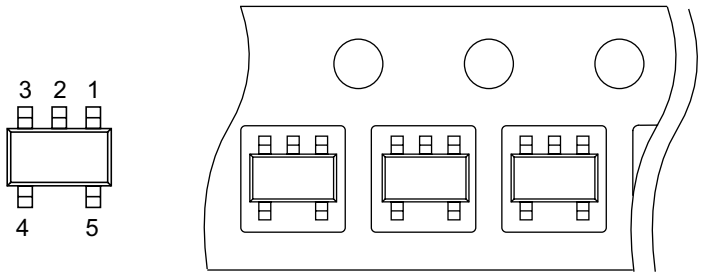
UNIT	mm
Seiko Instruments Inc.	

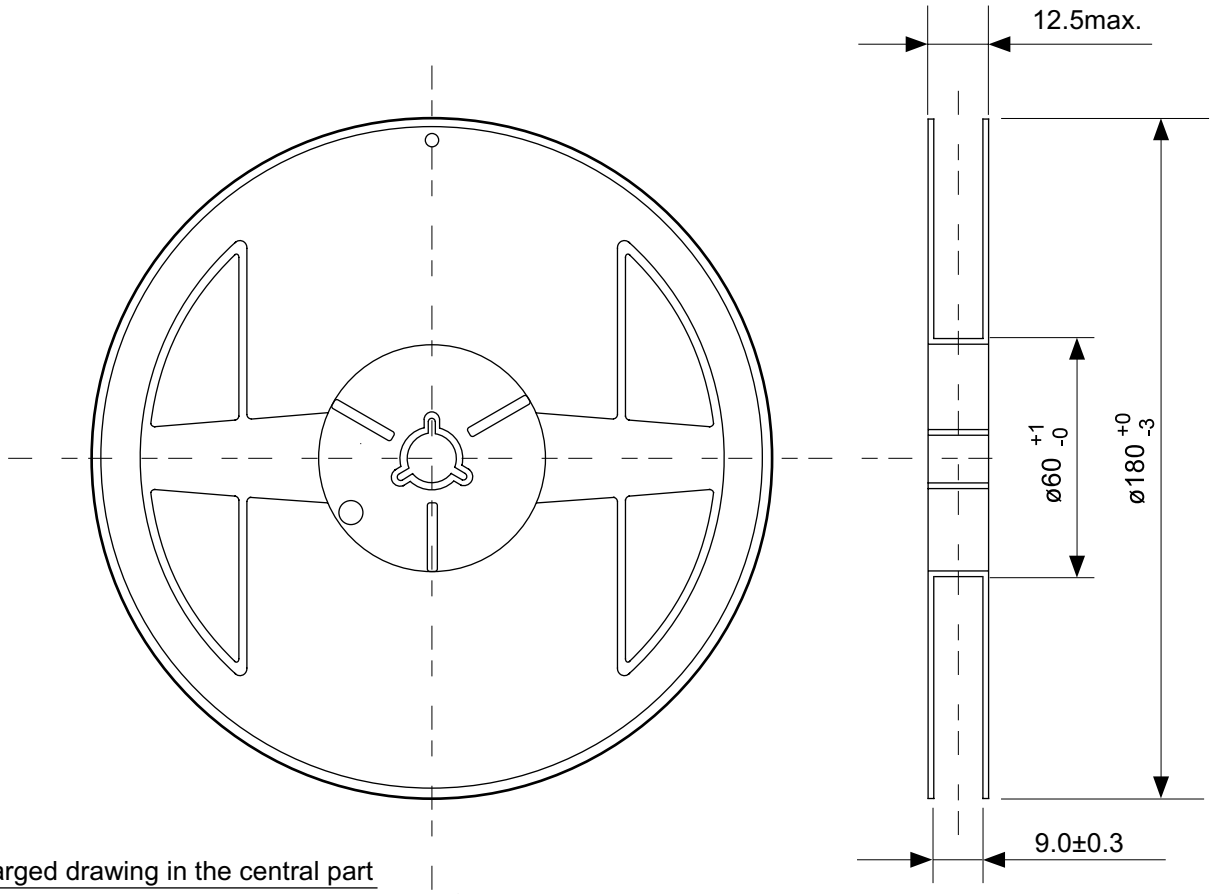




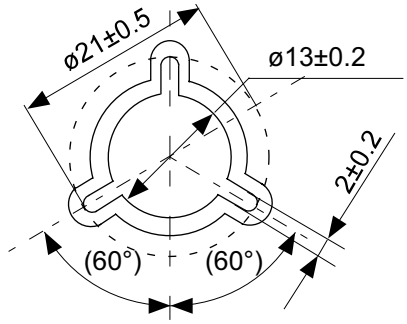
Feed direction

No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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