August 2014

FSA832 — USB 2.0 High-Speed (480 Mbps) Charger Detection IC with Isolation Switch

Features

USB Detection	USB Battery Charging Rev. 1.2 Supports Data Contact Detect (DCD) Dead Battery Provision (DBP) with 30-Minute Timer
Proprietary Charger and Other Detection	2.7 V / 2.0 V on DP/DM DP/DM Floating PS/2 Port Detection
Switch Type	Isolation Switch Closes for Charging Downstream Port (CDP) Standard Downstream Port (SDP)
V_{BUS}	28 V Over-Voltage Tolerance -2 V Under-Voltage Tolerance
Package	10-Lead MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch
Ordering Information	FSA832L10X

Applications

- MP3, Mobile Internet Device (MID), Cell Phone, PDA, Digital Camera, Notebook, and Netbook

Description

The FSA832 is a charger detection IC with an integrated isolation switch for use with micro/mini USB port. The FSA832 detects USB battery chargers and is compliant with USB Battery Charging Specification, Rev 1.2 (BC1.2).

The FSA832 also detects proprietary chargers that pull the USB data lines HIGH (2.7 V / 2.0 V), floating data lines, and PS/2 ports. The device determines if a charger, either through a Dedicated Charging Port (DCP) or Charging Downstream Port (CDP), is connected or if a typical PC host, a Standard Downstream Port (SDP), is connected. The FSA832 conforms to all the constraints for the Dead Battery Provision (DBP) within the BC1.2 specification, including a 30-minute timer that cannot exceed 45 minutes per BC1.2.

Typical Application

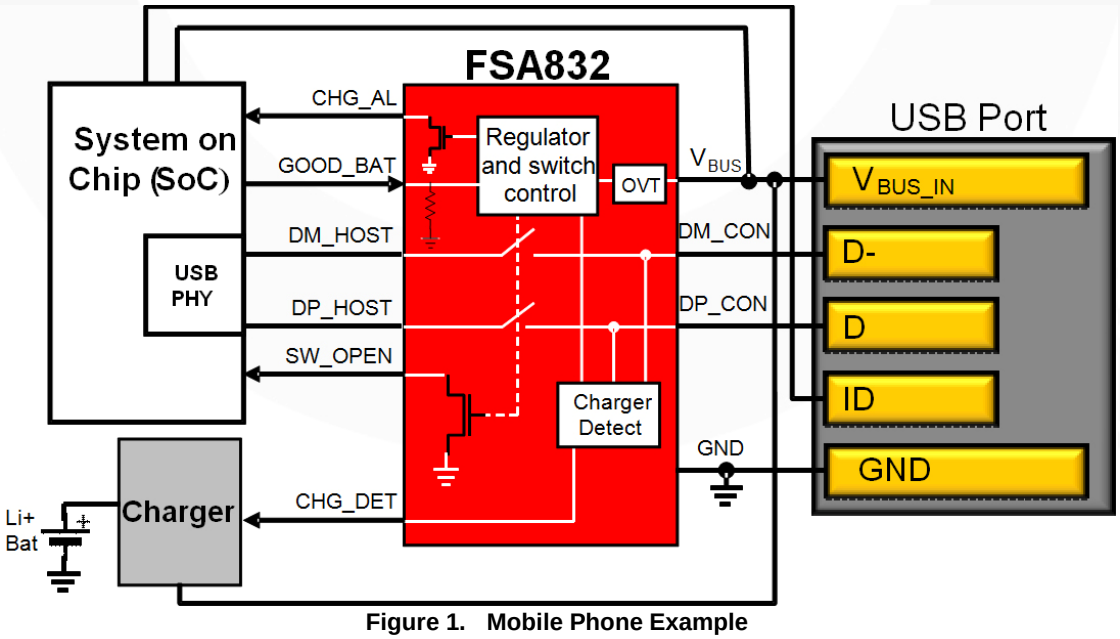


Figure 1. Mobile Phone Example

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package Description	Packing Method
FSA832L10X	-40 to 85°C	ZY	10-Lead, MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch	Tape & Reel

Pin Configurations

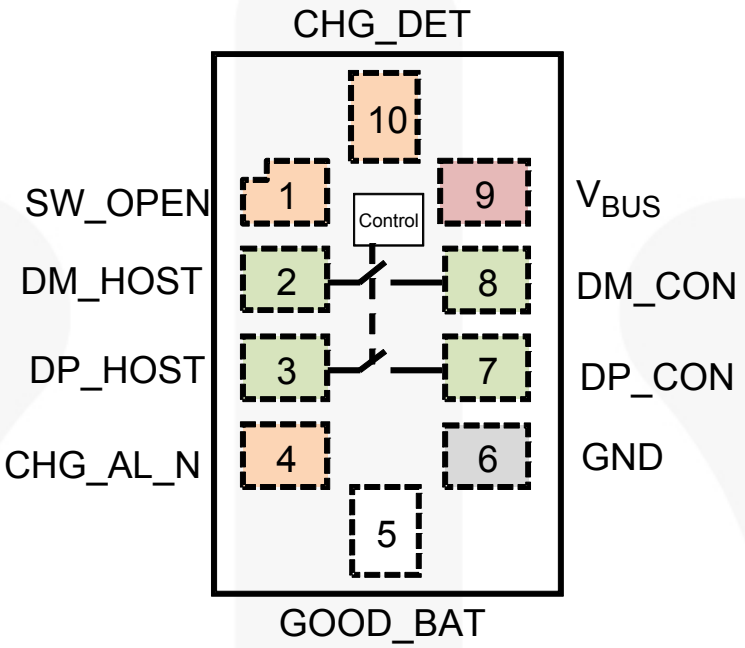


Figure 2. Pin Assignments (Top View)

Pin Descriptions

Name	Pin #	Description
USB Interface		
DP_HOST	3	D+ signal connected to the resident USB transceiver on the phone.
DM_HOST	2	D- signal connected to the resident USB transceiver on the phone.
Connector Interface		
V_{BUS}	9	Input voltage supply pin to be connected to the V_{BUS} pin of the USB connector.
GND	6	Ground
DP_CON	7	Connected to the USB connector D+ pin
DM_CON	8	Connected to the USB connector D- pin
Status Outputs		
CHG_DET	10	CMOS push/pull output connected to charger IC to indicate if a charger has been detected (LOW=charger not detected; HIGH=proprietary charger, DCP, or CDP charger detected).
SW_OPEN	1	Open-drain output pin; requires pull-up resistor to I/O voltage supply (LOW=switch closed; Hi-Z=switch open).
CHG_AL_N	4	CMOS open-drain output pin (LOW=V_{BUS} is valid and charge is allowed to be drawn from V_{BUS}; Hi-Z=V_{BUS} is not at a valid voltage).
Input Pin		
GOOD_BAT	5	Input that indicates if the battery is a good battery or a dead battery (V_{IL}=dead battery; V_{IH}=good battery).

Note:
1. Output voltage conditions are LOW = V_{OL} and HIGH = V_{OH}.

Table 1. Functionality

Device Detected	GOOD_BAT	SW_OPEN	CHG_AL_N	CHG_DET	DP_HOST	DM_HOST	DP_CON	DM_CON
DCP	X	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V_{DP_SRC}(2)	Hi-Z(2)
Proprietary Charger	X	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	Hi-Z	Hi-Z
CDP	HIGH	LOW	LOW	HIGH	DP_CON	DM_CON	DP_HOST	DM_HOST
CDP	LOW	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V_{DP_SRC}	Hi-Z
PS/2 Ports(3)	X	Hi-Z	LOW	LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SDP	HIGH	LOW	LOW	LOW	DP_CON	DM_CON	DP_HOST	DM_HOST
SDP	LOW	Hi-Z	LOW	LOW	Hi-Z	Hi-Z	V_{DP_SRC}	Hi-Z
SDP, CDP, or DCP plugged in and after 30-minute timer expires	LOW	Hi-Z	Hi-Z	LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z
V_{BUS} < V_{BUS} valid to V_{BUS} > V_{BUS} valid operation prior to completing detection of SDP, CDP, or DCP. Upon detection, all outputs switch as in rows above.	X	Hi-Z	Hi-Z	Hi-Z to LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note:
2. Hi-Z is the internal state of DM_CON. Since a DCP has been detected, DM_CON is shorted to DP_CON externally and DM_CON is shorted to V_{DP_SRC}. V_{DP_SRC} is not put on DP_CON for proprietary chargers.
3. DP_CON and DM_CON are pulled to V_{BUS} through a resistor by the PS/2 port when it is connected to the FSA832.

Functional Description

Data Contact Detect (DCD)

DCD relies on the D+ and D- lines being present. DCD waits until the internal timeout t_{DCD_TOUT} has expired in the following cases:

- If a charger does not have a D+ pin on the USB connector;
- If the D+ pin is not shorted to D- pin on the connector,
- If D+ is pulled up to a supply; or
- If D+ does not have a sufficient path to ground to defeat a pull-up IDP_SRC (I_{DP_SRC}) current source.

The FSA832 proceeds with charger detection even though it is unlikely that a charger is present. If there is no charge, the algorithm reports an SDP and closes the switch. If a device is pulling D+ HIGH, this voltage presents itself to the USB transceiver or Physical Layer Interface (PHY) block within a System on Chip (SoC) after the switch is closed.

If the DCD timeout is insufficient and the PHY block is so equipped, DCD and the charging algorithm can be repeated in the PHY block. The stipulation is that the total time from V_{BUS} valid to USB transceiver connection with a 1.5 kΩ pull-up to 3.3 V must be one (1) second, per USB 2.0 standards, provided the portable device does not have a dead battery.

CHG_AL_N Output and Output Timing

CHG_AL_N output indicates that charge is allowed to be drawn from V_{BUS} when CHG_AL_N is LOW. When the FSA832 first powers up and prior to detection, the CHG_AL_N pin can follow V_{BUS} up to 28 V, which is the absolute maximum V_{BUS} voltage allowed. Whenever V_{BUS} is at GND, the FSA832 is completely off and the switches and all I/Os are in the Hi-Z state. When V_{BUS} climbs above the valid V_{BUS} threshold, detection occurs automatically and CHG_DET, SW_OPEN, and CHG_AL_N all simultaneously switch to the states indicated in Table 1 if GOOD_BAT is HIGH *(see Dead Battery Provision description for GOOD_BAT = LOW).*

Dead Battery Provision

BC1.2 and USB 2.0 allow a portable device (defined as a device with a battery) with a dead battery to take a maximum of 100 mA from the USB V_{BUS} line for a maximum of 45 minutes as long as the portable device forces the D+ line to V_{DP_SRC}. The FSA832 starts detection when V_{BUS} crosses the V_{BUSVLD} threshold and, if it detects a CDP or SDP and GOOD_BAT is HIGH, automatically closes the switch and does not force the DP_CON pin to V_{DP_SRC}.

Once charger detection is complete, the FSA832 starts a 30-minute timer and forces the DP_CON pin to V_{DP_SRC} until the timer elapses. During the 30-minute period; if GOOD_BAT is LOW, V_{DP_SRC} is applied to DP_CON and the D+/D- switches are opened. If GOOD_BAT is HIGH, V_{DP_SRC} is not applied to DP_CON and the D+/D- switches are closed. If GOOD_BAT is LOW when the 30-minute timer expires; regardless of whether a proprietary charger, SDP, CDP, or DCP was previously detected; the FSA832 removes V_{DP_SRC} from DP_CON and forces CHG_DET LOW and CHG_AL_N to Hi-Z (SW_OPEN remains in Hi-Z). To exit this fault condition, remove V_{BUS}, wait for all the V_{BUS} Printed Circuit Board

(PCB) capacitance to discharge, and re-apply V_{BUS}. Table 1 provides the functionality of the pins when the timer expires.

When GOOD_BAT is HIGH and the battery is removed from the portable device while V_{BUS} is valid, bringing GOOD_BAT LOW; the FSA832 opens the isolation switches on DP_CON and DM_CON and forces the DP_CON pin to V_{DP_SRC}. In this scenario, the timer generally expires because the SoC does not have a supply to bring GOOD_BAT HIGH unless the battery that was removed is re-inserted within 30 minutes after the USB plug is inserted.

If an SDP or CDP is inserted with GOOD_BAT HIGH during the 30-minute timer; then GOOD_BAT changes to LOW, SW_OPEN changes to Hi-Z, and the counter continues counting until the 30 minutes expires. If GOOD_BAT then returns to HIGH, SW_OPEN changes to LOW and finishes out the 30-minute time.

GOOD_BAT has an internal pull-down resistor to ensure it is LOW when the SoC is powered down. This input is designed to have very V_{IH} interface with low-voltage SoCs driven with 1.2 V supplies. GOOD_BAT can be connected to the processor supply voltage becauses the processor should wake up whenever V_{BUS} is turned on.

Proprietary Chargers

Chargers pulling the USB data line DM_CON HIGH to 2.0 V or 2.7 V and data line DP_CON HIGH to 2.0 V or 2.7 V are detected by the FSA832 and reported proprietary chargers with a higher charge current allowed. Other chargers that float the DP/DM lines are also detected as a proprietary by means of float detection. This allows a proprietary charger with floating DP/DM to benefit from higher charge current.

PS/2 Port

Mice and keyboards utilizing the PS/2 port interface pull the clock and data pins of the PS/2 connector HIGH to VBUS through a resistive pull-up. When the PS/2 device is adapted to a USB interface, the clock and data pins are translated to the DP_CON and DM_CON lines of the USB connector, respectively.

The benefit of detecting the PS/2 port as a separate device is the ability to limit the current that can be drawn from the bus, thus protecting the PS/2 port. Once the PS/2 port is detected, the DP_HOST and DM_HOST switches remain open to protect the USB PHY connected to DP_HOST and DM_HOST from voltages as high as V_{BUS}.

Ground Drops

When a DCP is detected, V_{DP_SRC} is forced on DP_CON provided GOOD_BAT is HIGH or GOOD_BAT is LOW and the DBP timer has not expired. When ~1.5 A is flowing into V_{BUS} and GND lines of the USB cable, the current can create substantial ground drops that lift the ground of the portable device. This drop adds to the voltage at the DP_CON pin as seen from the DCP D+ pin. For the maximum ground drop of 375 mV specified in the BC1.2 specification and for the maximum V_{DP_SRC} of 0.7 V; the voltage as seen by the DCP would be 1.075 V. Smart DCPs that rely on this voltage detection to determine attach and detach detection need to take this into account.

V_{BUS} Tolerance

When V_{BUS} rises, an internal Power-On Reset (POR) detects this voltage and prepares the FSA832 for charger detection.

V_{BUS} voltages up to 28 V can be tolerated by the V_{BUS} pin. V_{BUS} can tolerate voltages up to -2 V for cases where a charger is plugged in backwards.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BUS}	Voltage from USB Connector			-2	28	V
V_{SW}	USB Switch I/O Voltage (DP_CON, DM_CON, DP_HOST, DM_HOST)			-0.5	6.0	V
I_{SW}	USB Switch Current (DP_CON to DP_HOST, DM_CON to DM_HOST)			-30	+30	mA
$V_{I/O}$	Voltage from GOOD_BAT, CHG_AL_N, CHG_DET and SW_OPEN I/Os			-0.5	6.0	V
V_{CA}	Voltage from CHG_AL_N Output			-0.5	28.0	V
$I_{I/O}$	CHG_AL_N, CHG_DET and SW_OPEN Outputs Sink/Source Current			-5	+5	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System	USB Pins (DP_CON, DM_CON, V_{BUS})	Air Gap		15	kV
			Contact		8	
	Human Body Model, JEDEC JESD22-A114		All Pins		6	
	Charged Device Model, JEDEC JESD22-C101		All Pins		1	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	V_{BUS} Input HIGH Voltage	4	6	V
V_{SW}	Switch I/O Voltage for USB Path	0	3.6	V
T_A	Operating Temperature	-40	+85	ºC

DC Electrical Characteristics

Unless otherwise indicated, V_{BUS}=4 V to 6 V and T_A=-40 to +85°C. Typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Status Outputs						
V_{OHCD}	Output HIGH Voltage (CHG_DET)	I_{OH}=-2 mA	2.0			V
V_{OL}	Output LOW Voltage (CHG_DET, CHG_AL_N, SW_OPEN)	I_{OL}=2 mA			0.4	V
t_{DIFF}	Skew Between Any Output (CHG_DET, CHG_AL_N, SW_OPEN) Switching Relative to Other Outputs Switching	$I_{I/O}$=±2 mA, CHG_AL_N=20 kΩ to 5 V, SW_OPEN=10 kΩ to 1.8 V			100	ns
V_{BUS} Pin						
$VBUS_{VLD}$	V_{BUS} Valid Detection Threshold(4)		0.8		4.0	V
I_{BUSIN}	V_{BUS} Input Leakage	V_{BUS}=0 V to 0.8 V			3	µA
$I_{VBUSACT}$	V_{BUS} Active Mode Average Current	USB Path Active, USB Switch Closed After Charger Detection			250	µA
t_{OUT}	Time from V_{BUS} Valid Asserted to CHG_DET, CHG_AL_N and SW_OPEN Outputs Valid for BC1.2 Standard Accessory Detection (SDP, DCP, or CDP)	DP_CON Pulled Down to GND with 15 kΩ; All Voltages Forced on V_{BUS}, DP_CON, DM_CON, and GND simultaneously			250	ms
Switch Characteristics						
I_{OFF}	Power Off Leakage Current	USB Path V_{BUS}=0 V, V_{SW}=0 V or 3.6 V, Figure 4			10	µA
R_{ONUSB}	High-Speed USB Range Switch On Resistance(4)	V_{DP_CON} / V_{DM_CON}=0 V, 0.4 V; I_{ON}=8 mA; Figure 3; V_{BUS}=4 V to 6 V		4.5	6.0	Ω
Control Input						
V_{IH}	Input HIGH Voltage (GOOD_BAT)		1.1			V
V_{IL}	Input LOW Voltage (GOOD_BAT)				0.5	V
R_{PD}	Pull-Down Resistance (GOOD_BAT)		1			MΩ
I_{IN}	Input Leakage Current (GOOD_BAT)	V_{BUS}=5 V, GOOD_BAT=0 V to 4.4 V			10	µA
I_{IOFF}	Off-State Leakage Current (GOOD_BAT)	V_{BUS}=0 V, GOOD_BAT=0 V to 4.4 V			10	µA
t_{DBP}	Dead Battery Provision (DBP) Timer		15	30	45	min
t_{GB}	Time from GOOD_BAT Asserted to SW_OPEN De-Asserted, Switches Closed and Meet the R_{ONUSB} Specification				30	ms
t_{DB}	Time from GOOD_BAT De-asserted to SW_OPEN Asserted, Switches Opened				65	ms
Battery Charger Detection Parameters from BC1.2 Specification						
V_{DAT_REF}	Data Detect Voltage		0.25		0.40	V
V_{DM_SRC}	D- Source Voltage(5)		0.5		0.7	V
V_{DP_SRC}	D+ Source Voltage(5)		0.5		0.7	V
V_{LGC}	Logic Threshold		0.8		2.0	V
I_{DM_SINK}	D- Sink Current		25		175	µA
I_{DP_SINK}	D+ Sink Current		25		175	µA
I_{DP_SRC}	Data Contact Detect Current Source		7		13	µA

Continued on the following page…

DC Electrical Characteristics

Unless otherwise indicated, V_{BUS}=4 V to 6 V and T_A=-40 to +85°C. Typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{DCD_DBNC}	Data Contact Detect Debounce		10			ms
t_{DCD_TOUT}	Time for DCD to Timeout		300	450	900	ms
t_{VDPSRC_ON}	D+ Voltage Source On Time		40			ms
t_{VDMSRC_ON}	D- Voltage Source On Time		40			ms

Notes:

4. Guaranteed by characterization; not production tested.
5. The voltage source, V_{DP_SRC} / V_{DM_SRC}, is able to source at least 250 µA when the output voltage is in the specified range. This voltage source should not pull DP_CON / DM_CON below 2.2 V when DP_CON / DM_CON is pulled to a voltage of 3.0 V minimum or 3.6 V maximum with a resistance of 900 Ω minimum or 1575 Ω maximum.

AC Electrical Characteristics

Unless otherwise specified, values are at T_A=-40 to +85°C; all typical values are for V_{CC}=3.3 V at T_A=25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Figure
Xtalk	Active Channel Crosstalk, DP_COM to DM_CON[6]	F=1 MHz, RT=50 Ω, C_L=0 pF		-78		dB	Figure 6
		F=240 MHz, RT=50 Ω, C_L=0 pF		-36			
O_{IRR}	Off Isolation Rejection Ratio, DM_HOST to DM_CON, DP_HOST to DP_CON[6]	f=1 MHz, R_T=50 Ω, C_L=0 pF		-84		dB	Figure 5
		f=240 MHz, R_T=50 Ω, C_L=0 pF		-34			
BW	Bandwidth of Switch[6]	R_T=50 Ω		1.5		GHz	Figure 5

Note:

6. Guaranteed by characterization; not production tested.

Capacitance

Unless otherwise specified, values are at T_A=-40 to +85°C.

Symbol	Parameter	Condition	Typical	Unit	Figure
C_{OFF}	DP_CON, DM_CON Off Capacitance[7]	V_{BIAS}=0.2 V, f=1 MHz	3.2	pF	Figure 7
C_{ON}	DP_CON, DM_CON On Capacitance[7]	V_{BIAS}=0.2 V, f=1 MHz	5.8	pF	Figure 8

Note:

7. Guaranteed by characterization; not production tested.

Test Diagrams

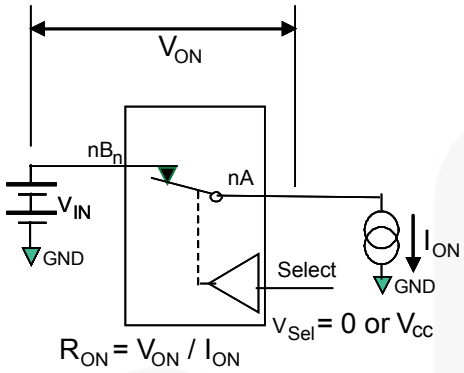
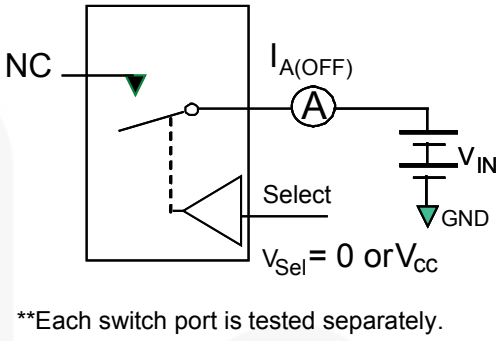


Figure 3. On Resistance



**Each switch port is tested separately.

Figure 4. Off Leakage

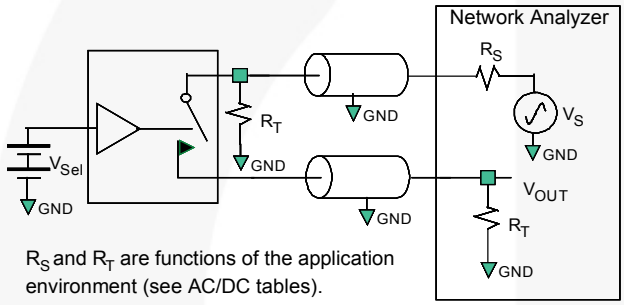


Figure 5. Channel Off Isolation

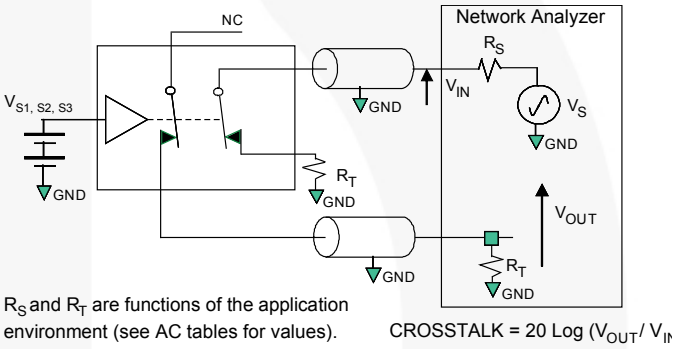


Figure 6. Active Channel Crosstalk

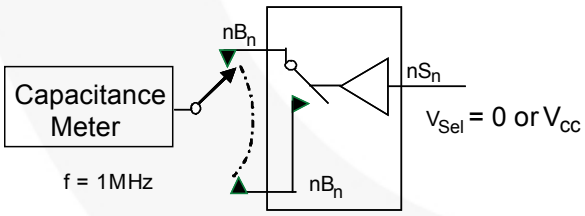


Figure 7. Channel Off Capacitance

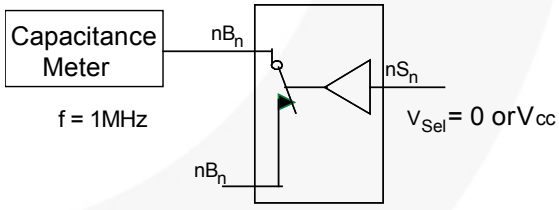
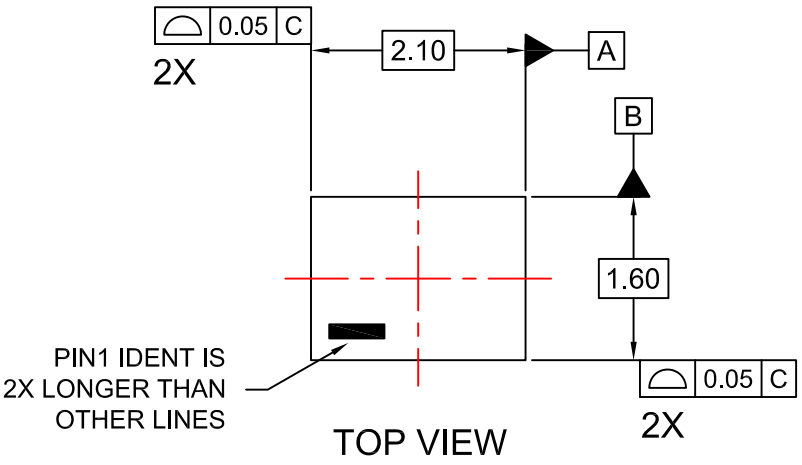
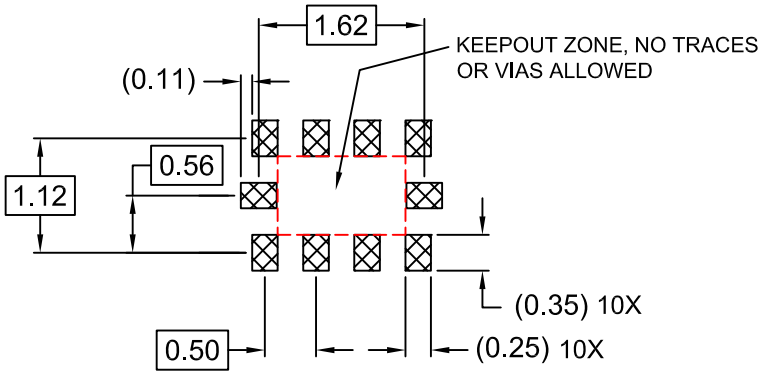


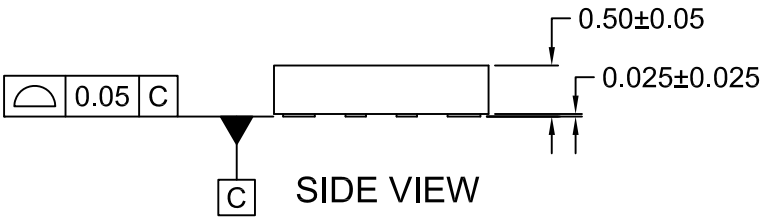
Figure 8. Channel On Capacitance



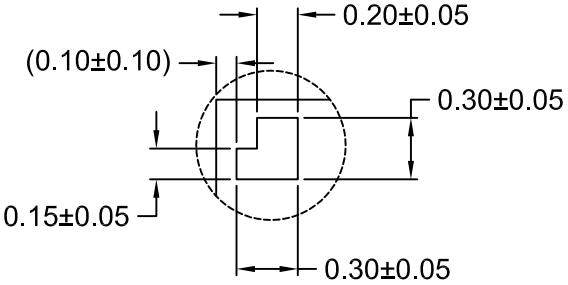
TOP VIEW



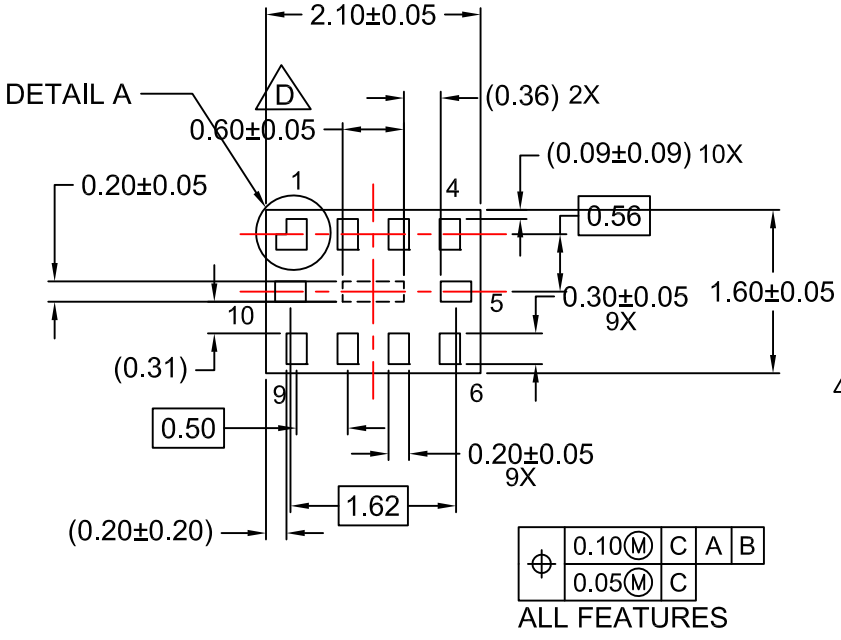
RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL A 2X SCALE



BOTTOM VIEW

NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD .

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.

E. DRAWING FILENAME: MKT-MAC10Arev6.

F. DIMENSIONS WITHIN ( ) ARE UNCONTROLLED

FAIRCHILD

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AttitudeEngine™
Awinda®
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource SM
GreenBridge™
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
MTi®
MTx®
MVN®
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
Power Supply WebDesigner™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™
Xsens™
仙童™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT HTTP://WWW.FAIRCHILDSEMI.COM. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

AUTHORIZED USE

Unless otherwise specified in this data sheet, this product is a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability. This product may not be used in the following applications, unless specifically approved in writing by a Fairchild officer: (1) automotive or other transportation, (2) military/aerospace, (3) any safety critical application – including life critical medical equipment – where the failure of the Fairchild product reasonably would be expected to result in personal injury, death or property damage. Customer's use of this product is subject to agreement of this Authorized Use policy. In the event of an unauthorized use of Fairchild's product, Fairchild accepts no liability in the event of product failure. In other respects, this product shall be subject to Fairchild's Worldwide Terms and Conditions of Sale, unless a separate agreement has been signed by both Parties.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Terms of Use

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I76